

Compal confidential

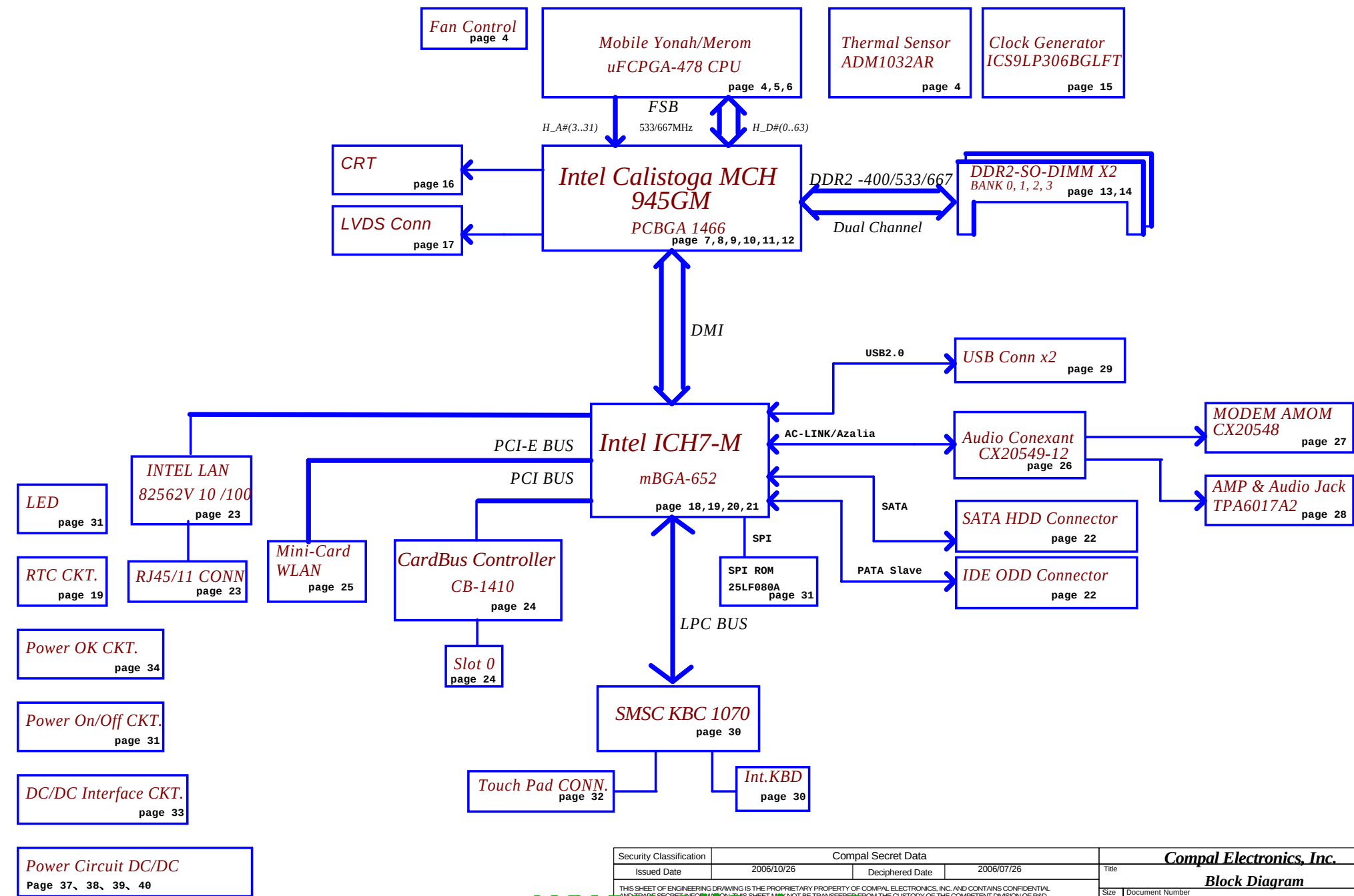
Schematics Document Mobile Yonah uFCPGA with Intel Calistoga_GM+ ICH7-M core logic

2007-03-20

REV:0.5

Security Classification		Compal Secret Data		Title	
Issued Date	2006/10/26	Deciphered Date	2006/07/26	Cover Sheet	
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Volga 2.0



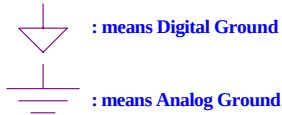
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Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (18.5V)	NA	NA	NA
B+	AC or battery power rail for power circuit	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VCCP	1.05V power rail for Processor I/O and MCH/ICH core power	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDRII Vtt	ON	OFF	OFF
+1.5VS	1.5V switched power rail for PCI-E interface	ON	OFF	OFF
+1.8V	1.8V power rail for DDRII	ON	ON	OFF
+2.5VS	2.5V switched power rail for MCH video PLL	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+RTC_VCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

Symbol Note :



NOXDP@ : means just build when XDP function disable.

LP@ : means just build when Low power clock gen. install

BATT@ : means need be mounted when 45 level assy or rework stage.

45@ : means need be mounted when 45 level assy or rework stage.

14@ : means need be mounted when 14.1"

WLAN@ : means need be mounted when have wireless LED Function

WLAN14@ : means need be mounted when have wireless LED Function and 14"

XDP@ : means just build when XDP function enable. When this time, docking PCI express will not work.

CONN@ : means ME parts

Debug@ : means Mini debug card use

Calistoga 945GM R3 SA0000059L0

Calistoga 945GM R1 SA0000059A0

Calistoga 940GML R3 SA000011C10

Calistoga 940GML R1 SA000011C00

ICH7 R3 SA00000V1A0

ICH7 R1 SA00000V1F0

IAT50 945GM FF 46147932L01

IAT50 940GML DF 46147932L02

IAT50 940GML DF 46147932L03 (No WLAN)

IAT60 945GM FF 46147932L21

IAT60 940GML DF 46147932L22

IAT60 940GML DF 46147932L23 (No WLAN)

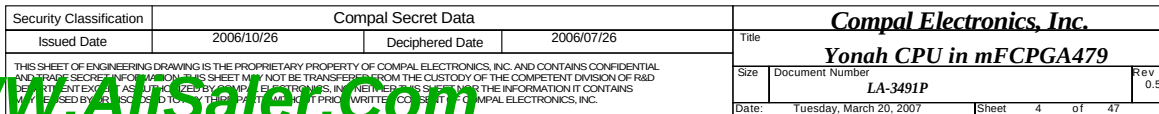
External PCI Devices

DEVICE	PCI Device ID	IDSEL #	REQ/GNT #	PIRQ
CARD BUS	D6	AD22	2	C

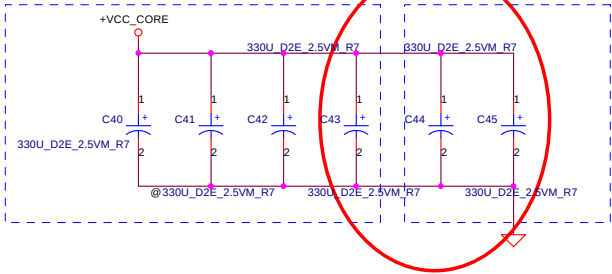
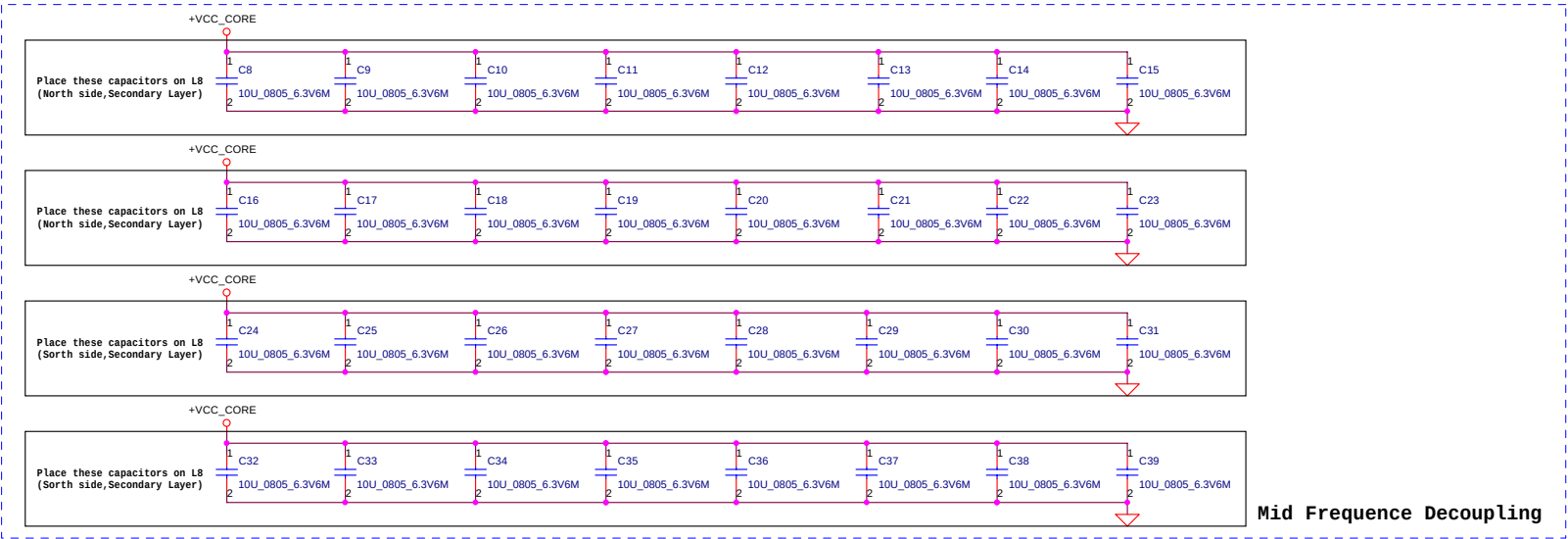
I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

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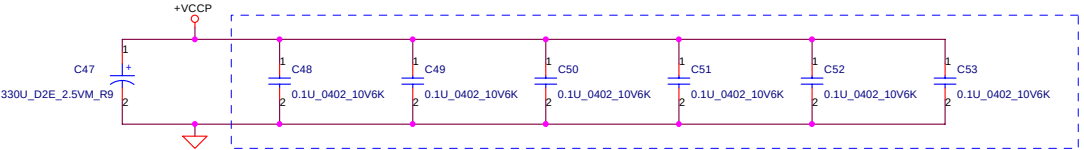


Security Classification	Compal Secret Data			Compal Electronics, Inc. Yonah CPU in mFCPGA479			
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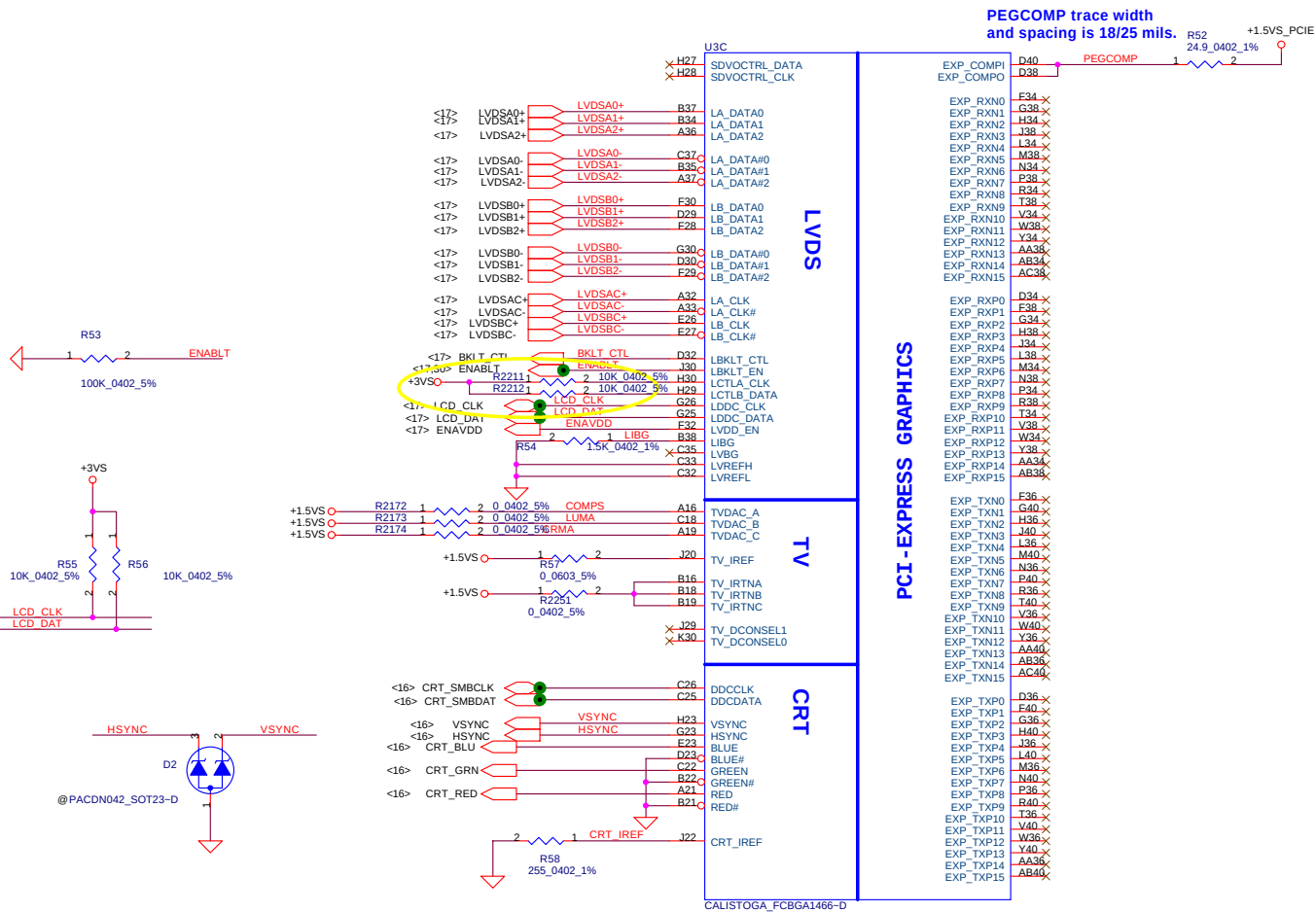
ESR <= 1.5m ohm
Capacitor > 1980uF

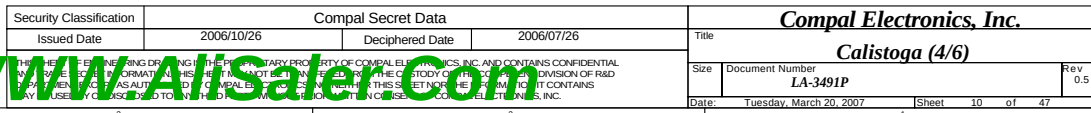
02/26 Change C43, C44, C45 to
1.9mm height for PV build short
term solution



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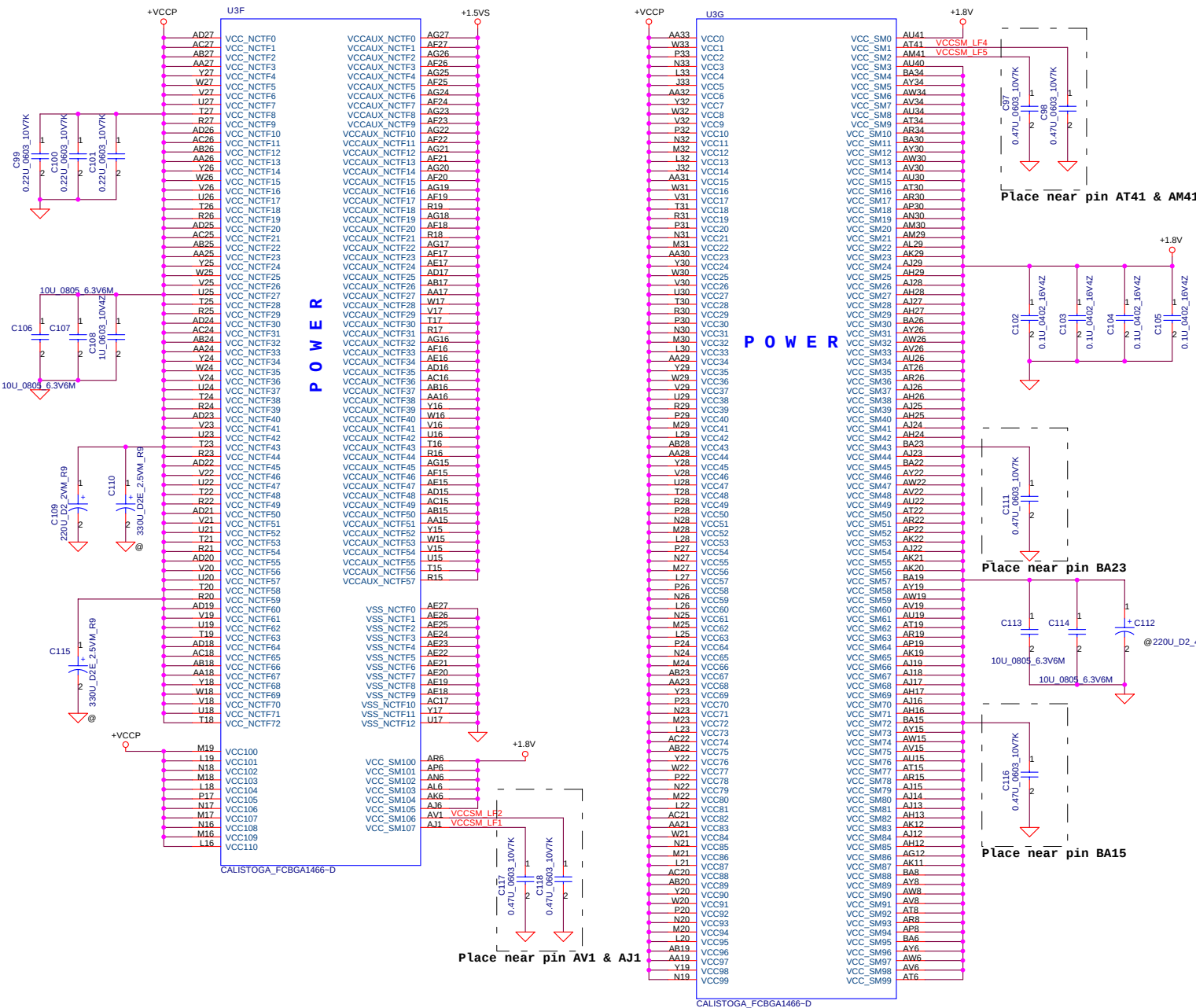
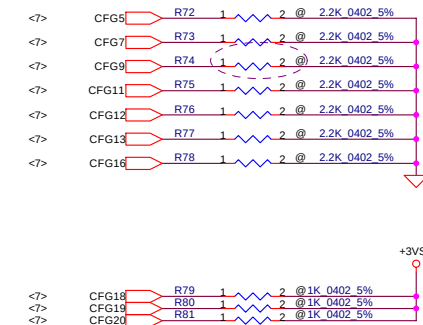


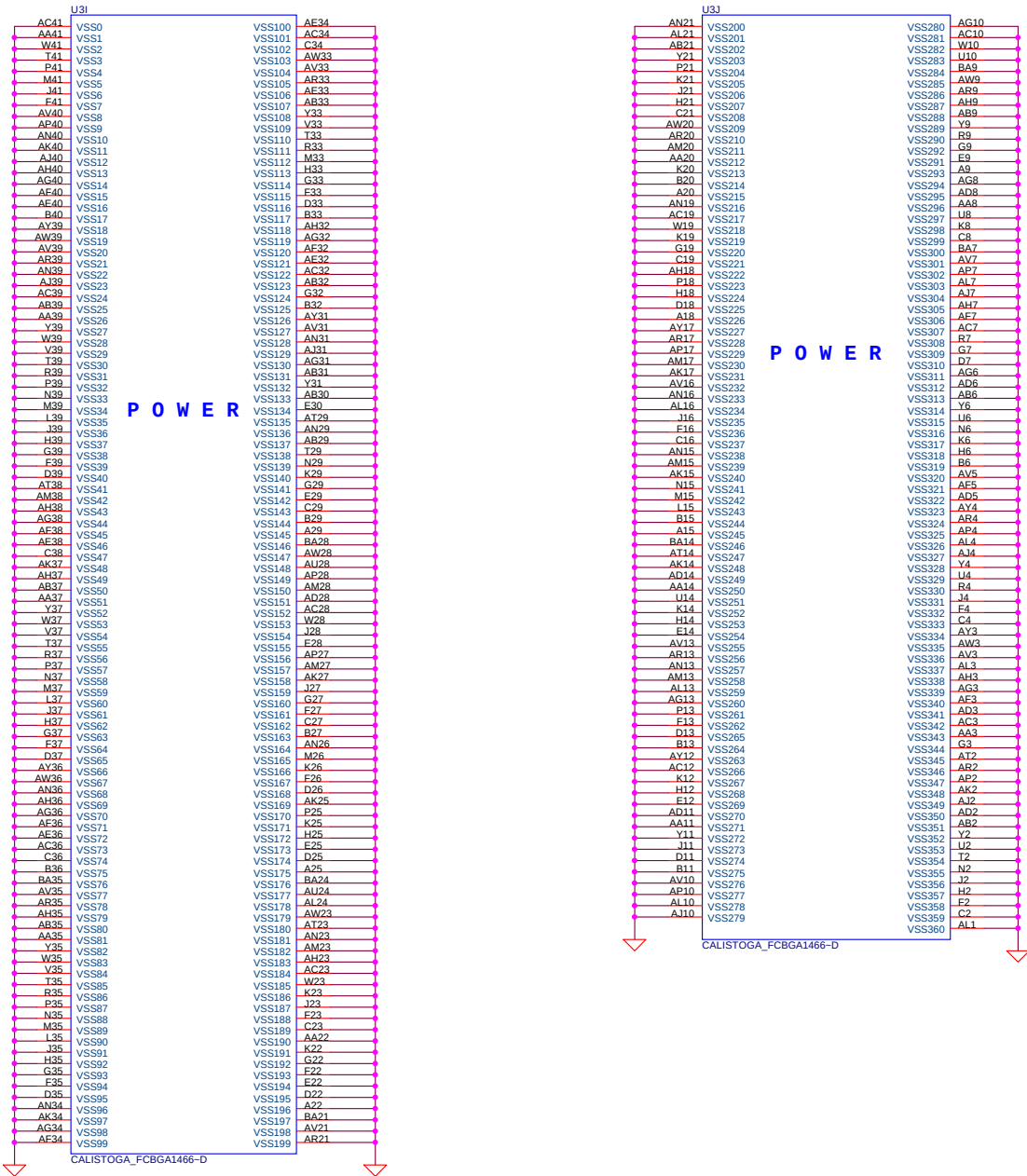


CFG[3:17] have internal pull up

CFG[19:18] have internal pull down

CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU *(Default)
CFG9	0 = Lane Reversal Enable * 1 = Normal operation *(Default)
CFG11	0 = Calistoga * (According to Intel Napa Schematic Checklist & CRB Rev1.301 document 2.2Kohm pull-down resistor required)
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG18	0 = 1.95V *(Default) 1 = 1.5V
CFG19	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present * (Default) 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. *(Default) 1 = PCIE/SDVO are operating simu.

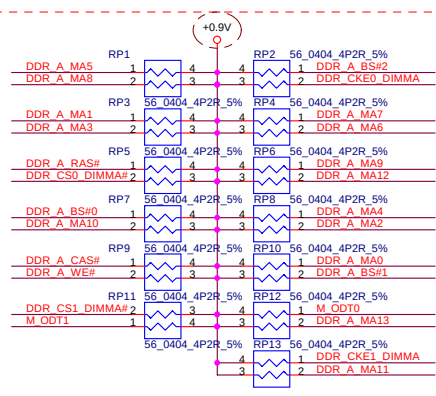




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The schematic shows a 10-bit DAC implemented with a resistor ladder. The power supply is +1.8V. The ladder is composed of 10 resistors, each with a value of 2.0U 0805 16V4Z. The nodes between the resistors are labeled C129, C128, C127, C126, C125, C124, C123, C122, C121, and C120. The output of the DAC is taken from node C120.

The diagram shows a 10-bit DAC implemented with a resistor ladder network. A +0.9V supply is connected to a series of resistors labeled C130 through C142. Each resistor is 0.1U 0402 1604Z. The resistors are connected in a ladder configuration, with the output of each stage connected to a common ground line.



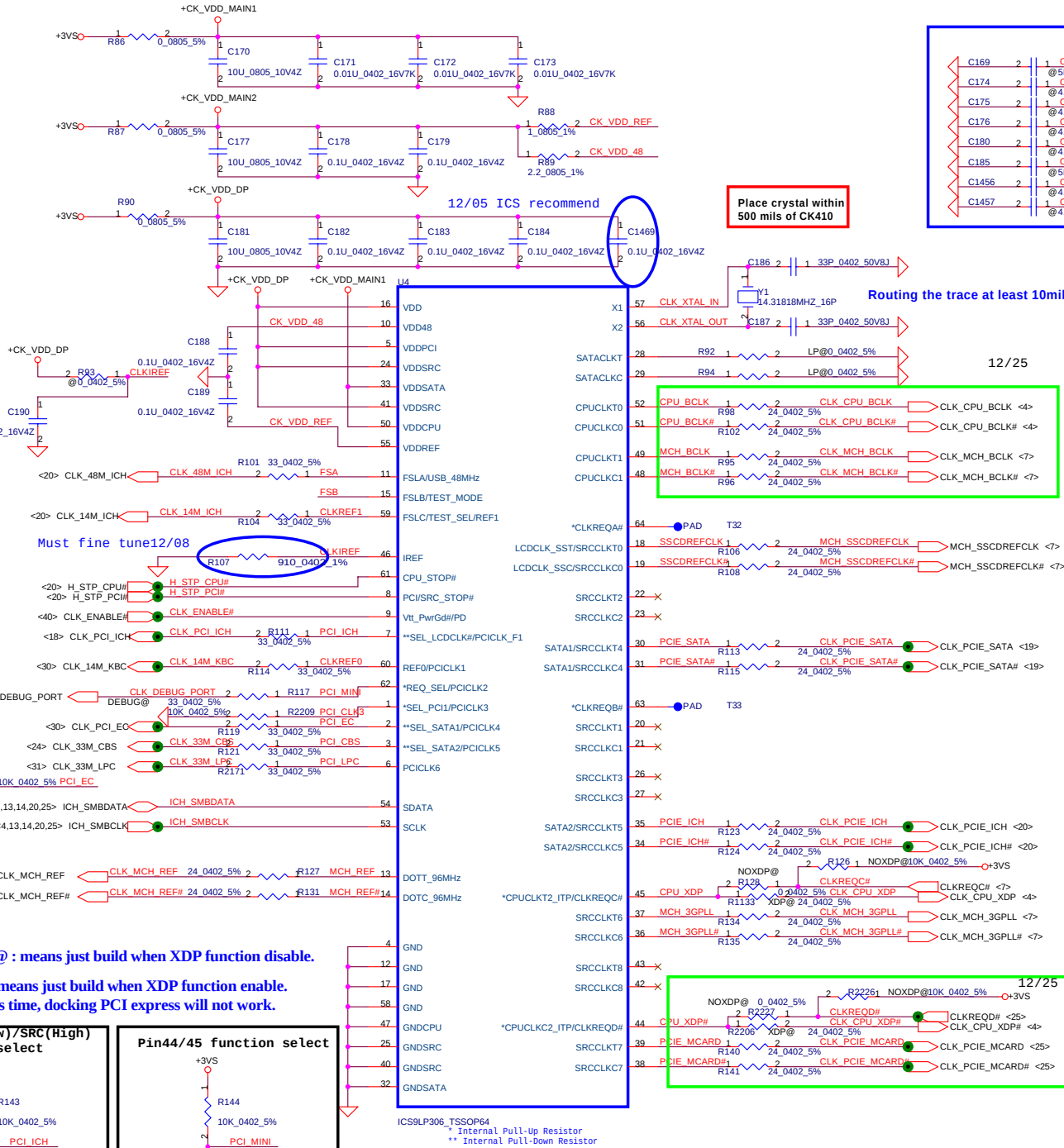
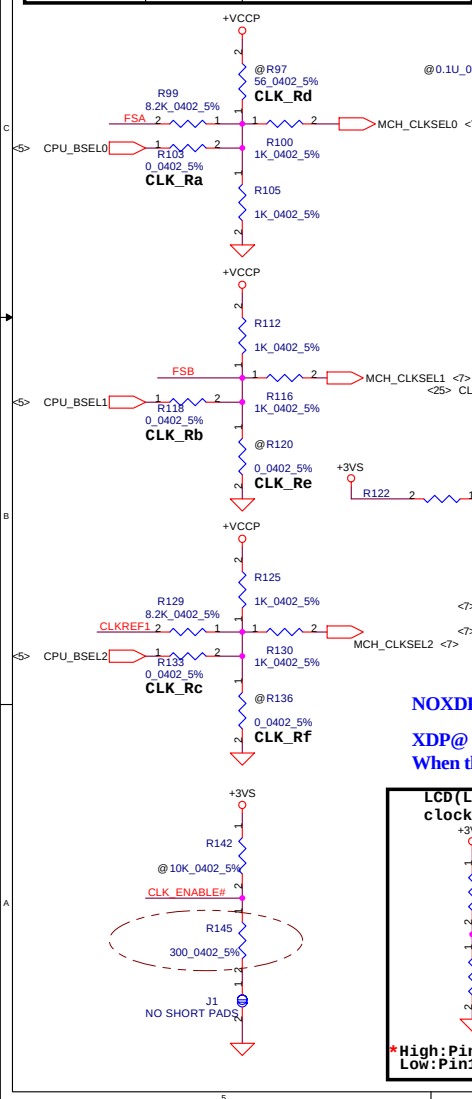
SO-DIMM A REVERSE
BOT side

Security Classification		Compal Secret Data		Compal Electronics, Inc. DDRII-SODIMM SLOT1	
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FSLC	FSLB	FSLA	CPU	SRC	PCI
------	------	------	-----	-----	-----

FSB Frequency Set:

CPU Driven * (Default)	Stuff	CLK_Ra	CLK_Rb	CLK_Rc
	No Stuff	CLK_Rd	CLK_Re	CLK_Rf
533MHz	Stuff	CLK_Rd	CLK_Re	CLK_Rf
	No Stuff	CLK_Ra	CLK_Rb	CLK_Rc
667MHz	Stuff	CLK_Rd		
	No Stuff	CLK_Ra	CLK_Rb	CLK_Rc
		CLK_Re	CLK_Rf	



XDP@ : means just build when XDP function enable.
When this time, docking PCI express will not work.

LCD(Low)/SRC(High)
clock select

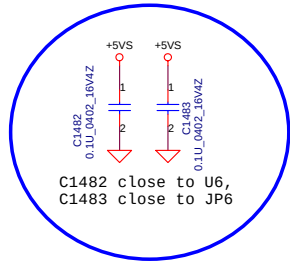
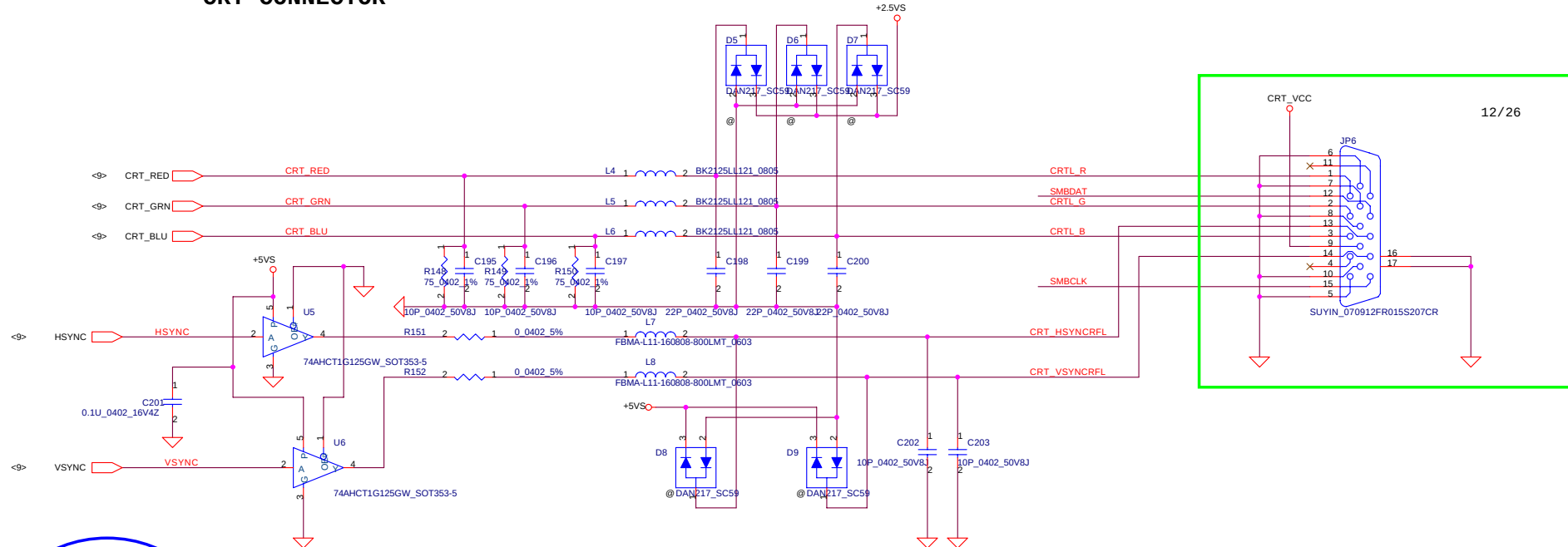
* High: Pin18/19 = 100MHz
Low: Pin18/19 = 96MHz

Pin44/45 function select

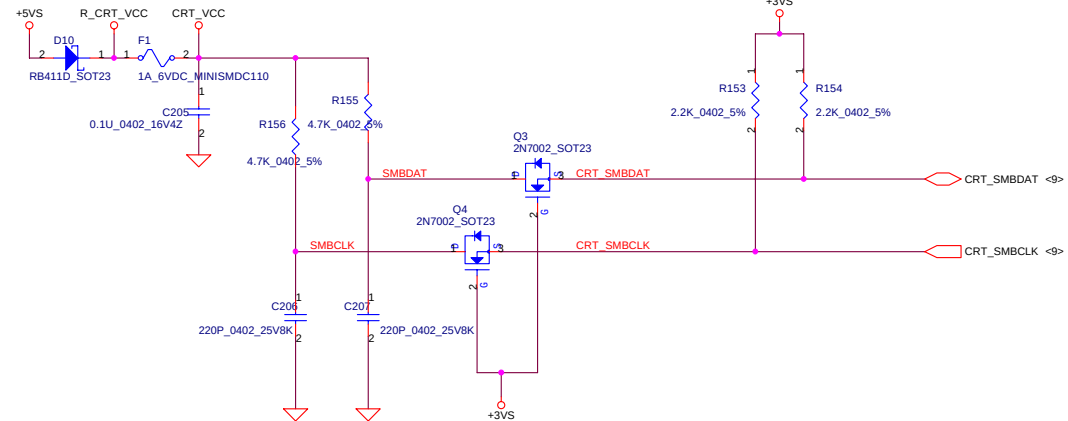
High: Pin44/45 = CLKREQ#
* Low: Pin44/45 = CPUCLK#

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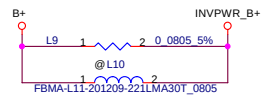
CRT CONNECTOR



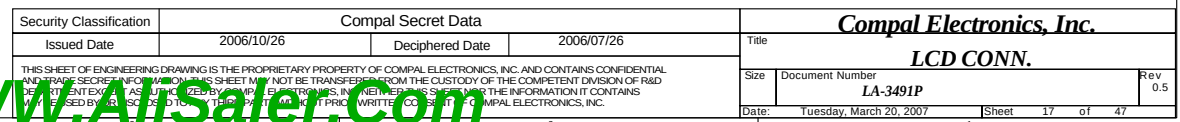
0119 HSYNC, VSYNC reference +5VS

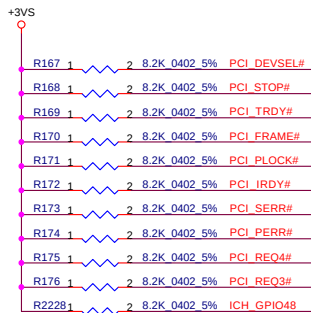


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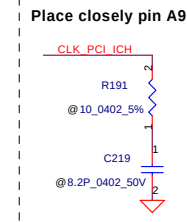
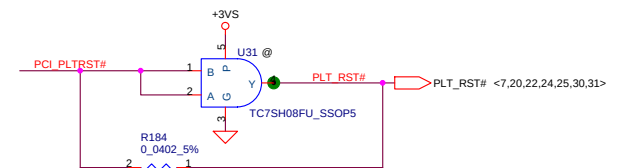
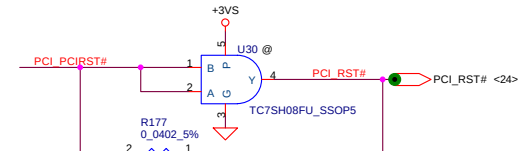
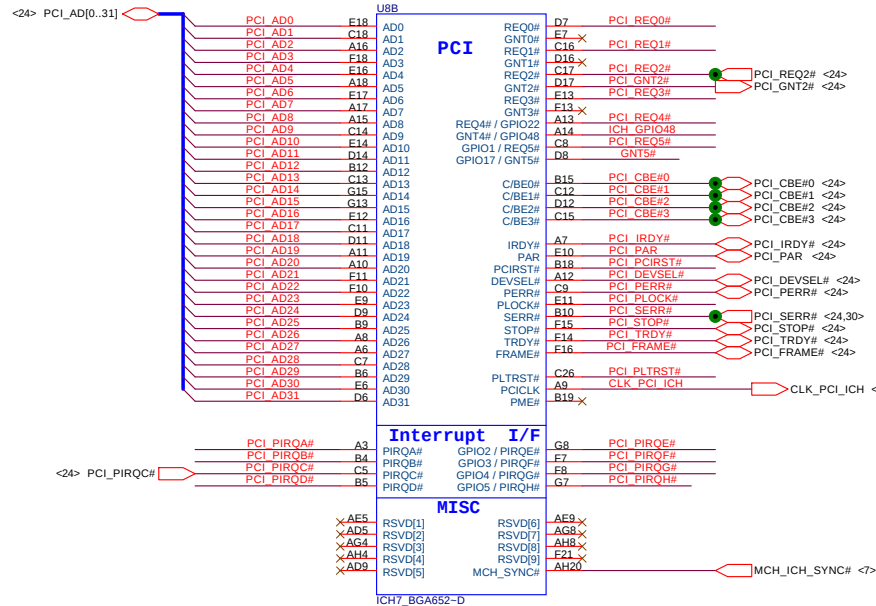
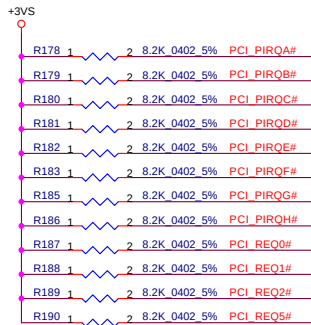


LCD/PANEL BD. CONN.





Change to RP before SI phase



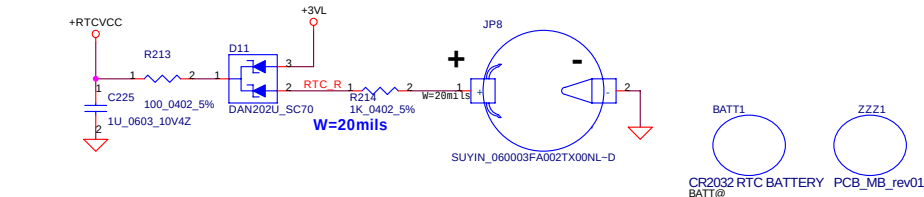
GNT5# and GNT4# have internal pull high 20K

Boot BIOS destination

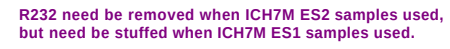
GNT5#	GNT4#	
0	1	SPI@ (Default)
1	0	PCI@
1	1	LPC@

The pad must be placed on PCB easily contact space for BIOS team setting.

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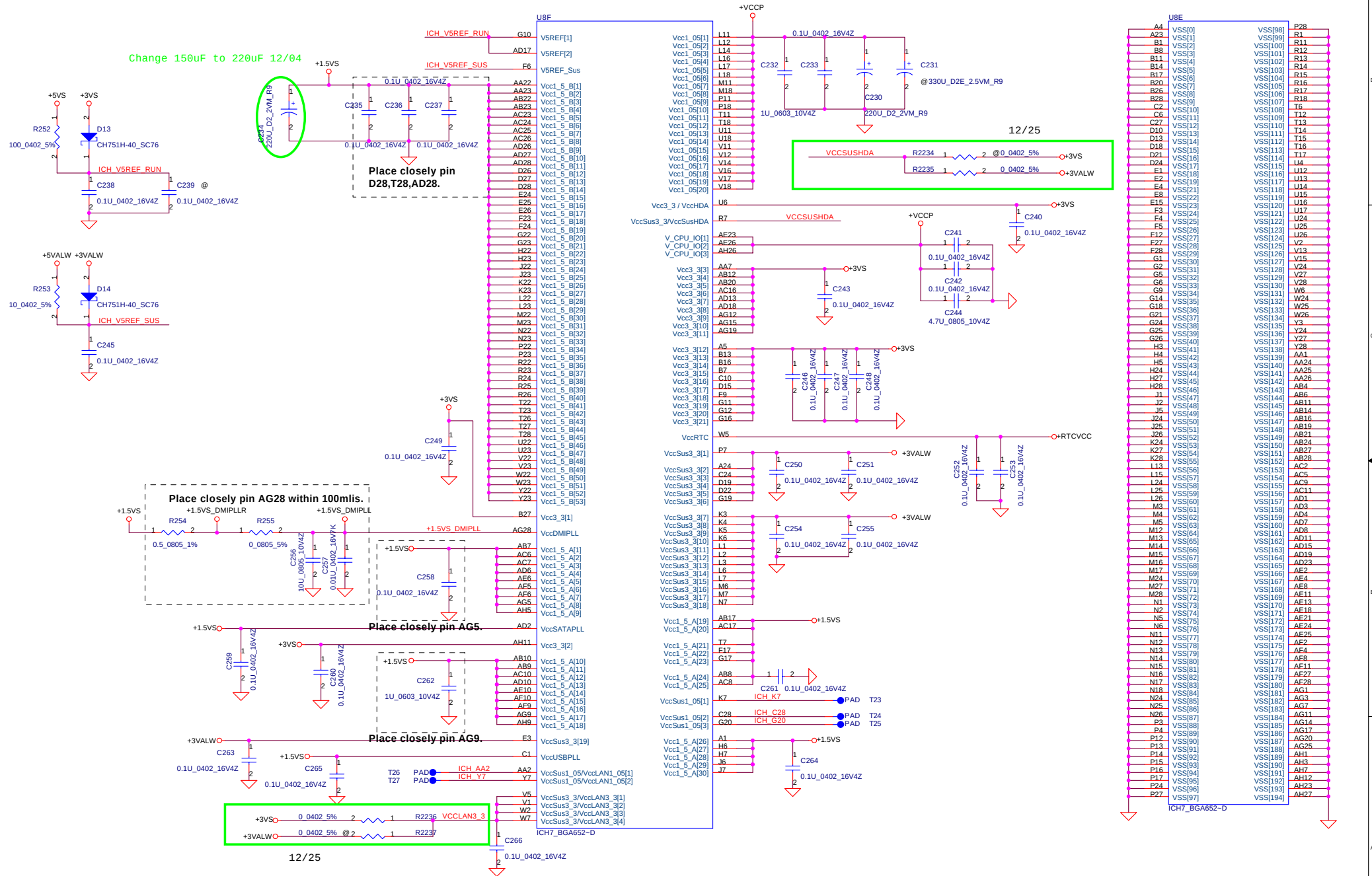


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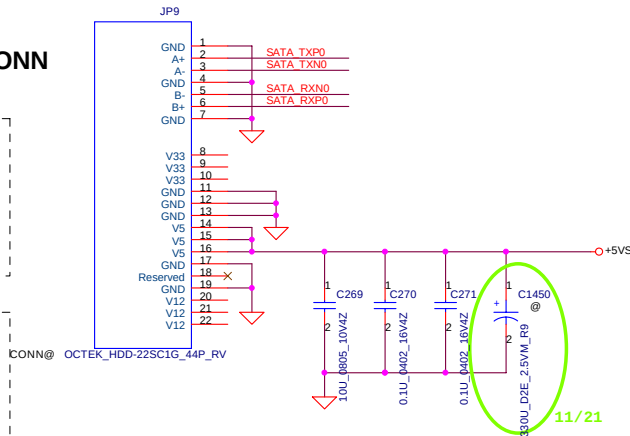
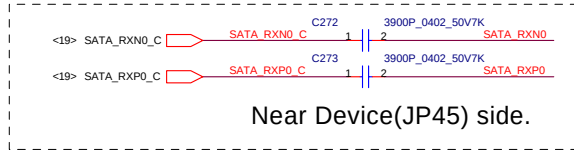
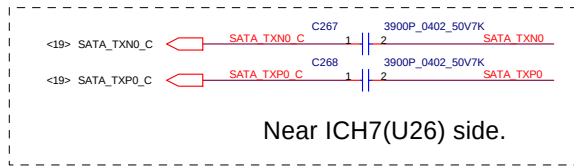
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Change 150uF to 220uF 12/04

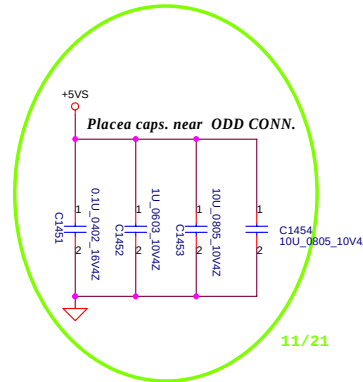
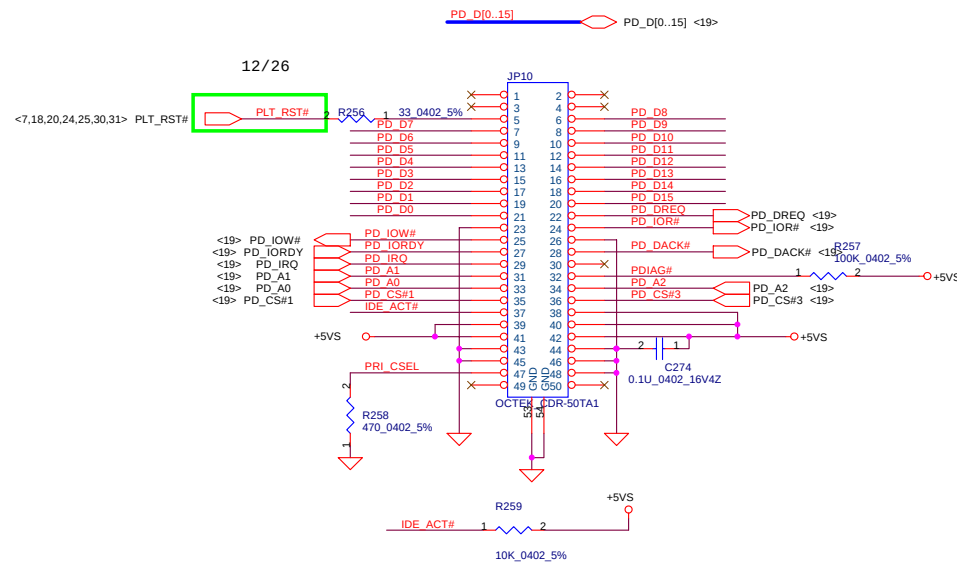


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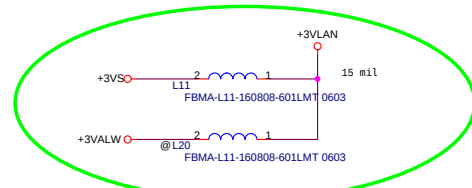
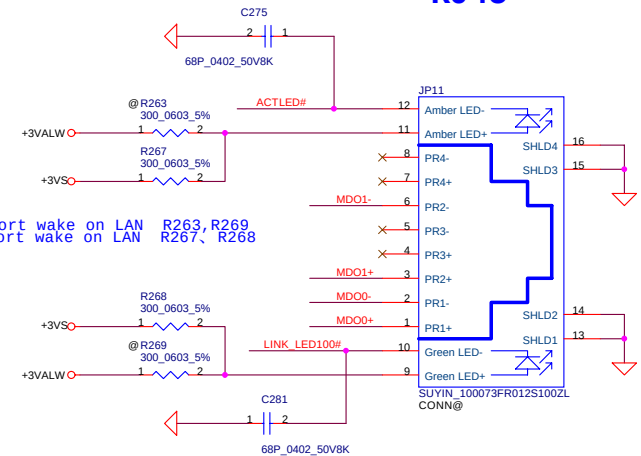
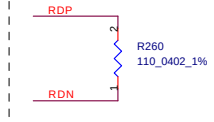
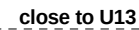
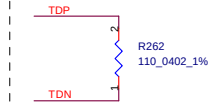
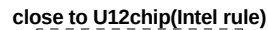
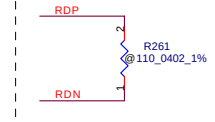
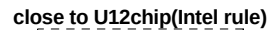
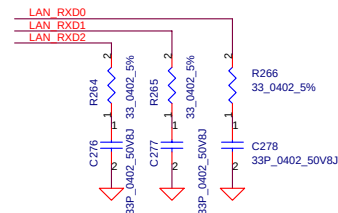
SATA CONN



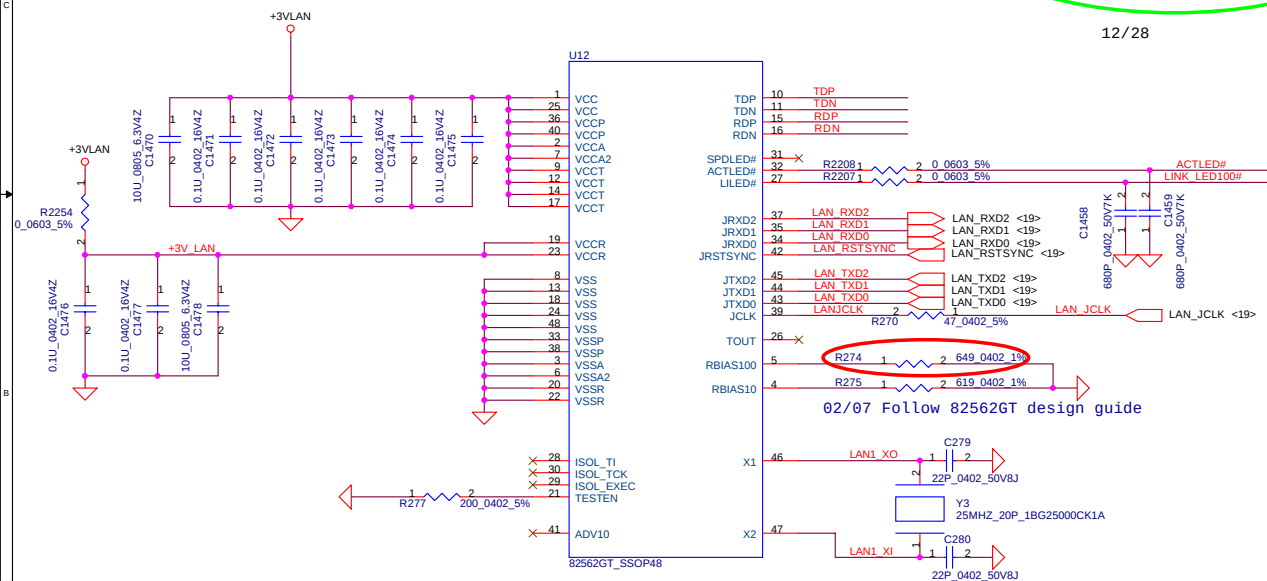
CD-ROM Connector



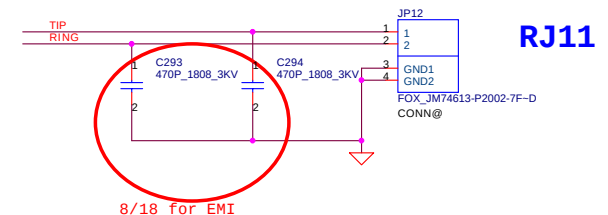
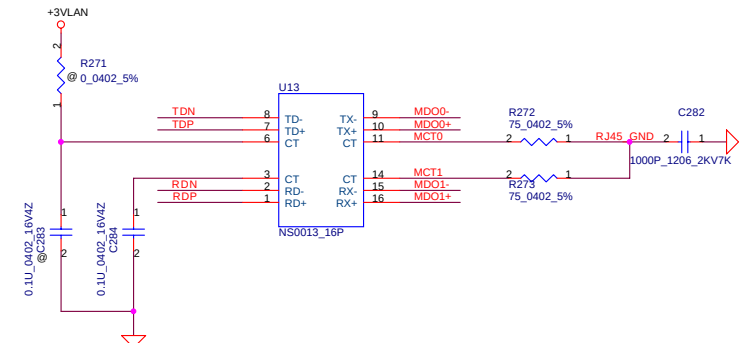
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Issued Date	2006/10/26	Deciphered Date	2006/07/26	HDD & ODD	
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				LA-3491P	Rev 0.5
				Date:	Tuesday, March 20, 2007
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12/28



02/07 Follow 82562GT design guide

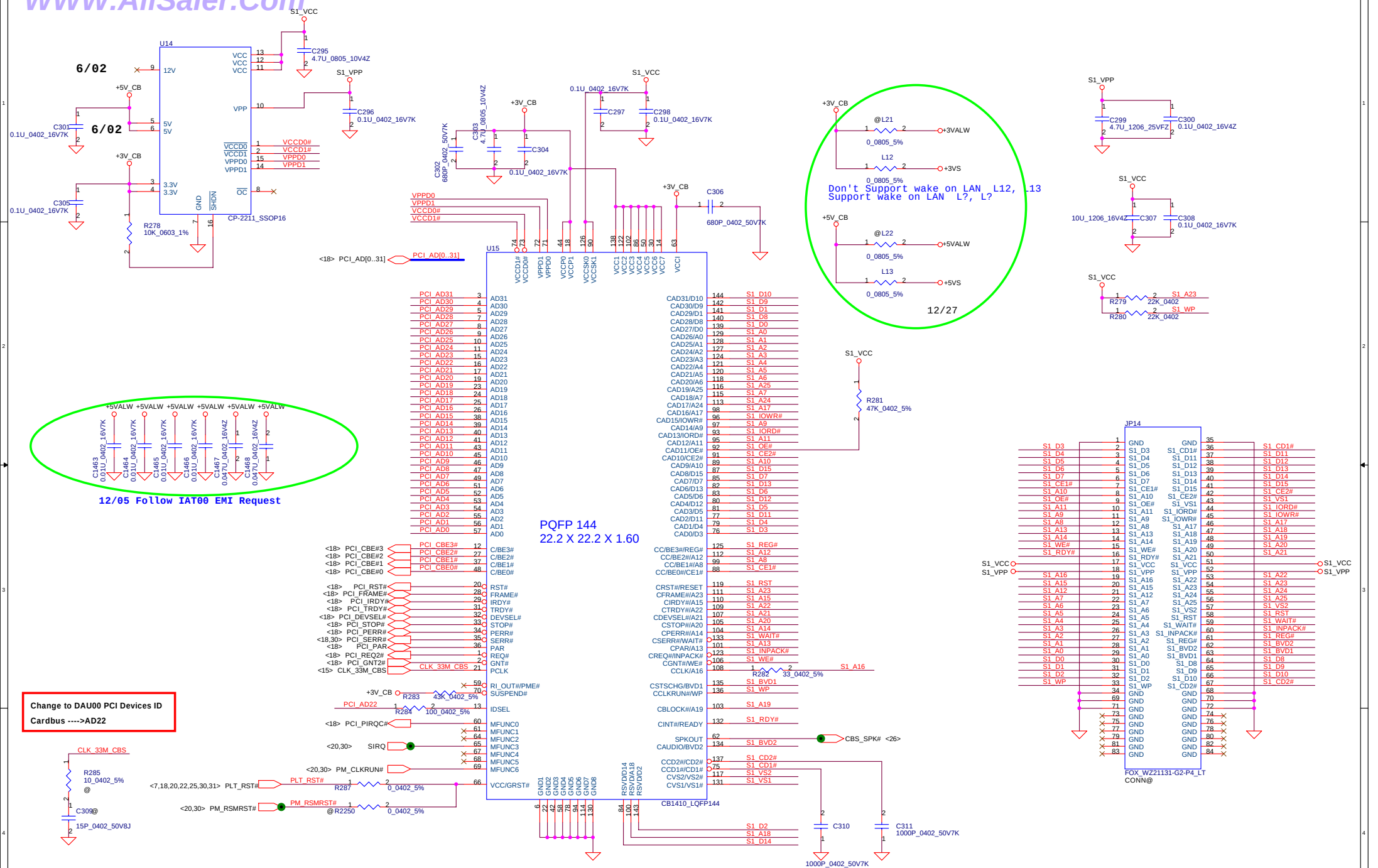


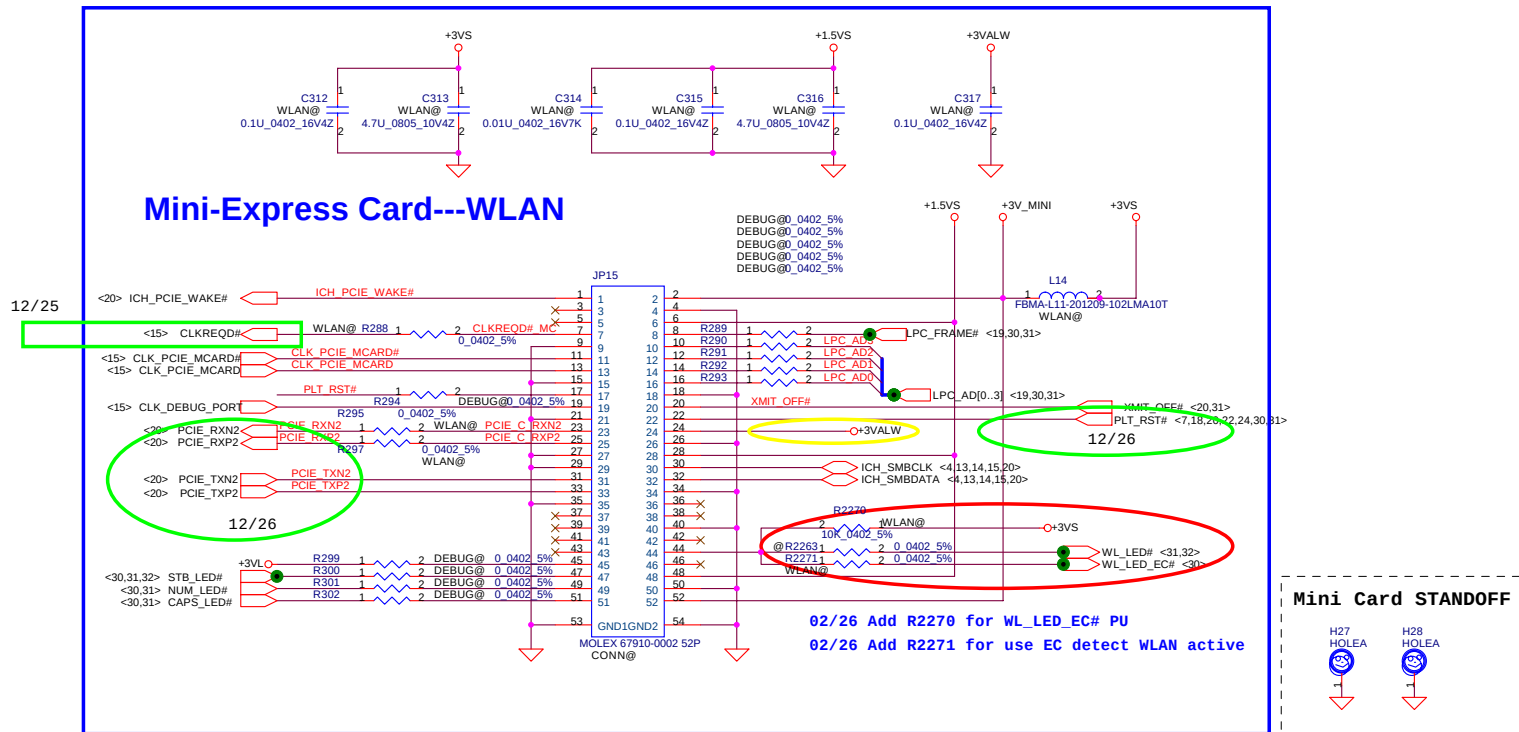
8/18 for EMI



JP13
RING
TIP
1
2
ACES_85205-0200
CONN@

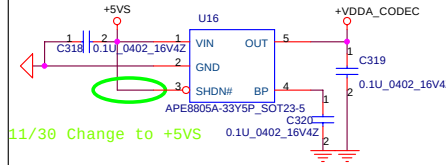
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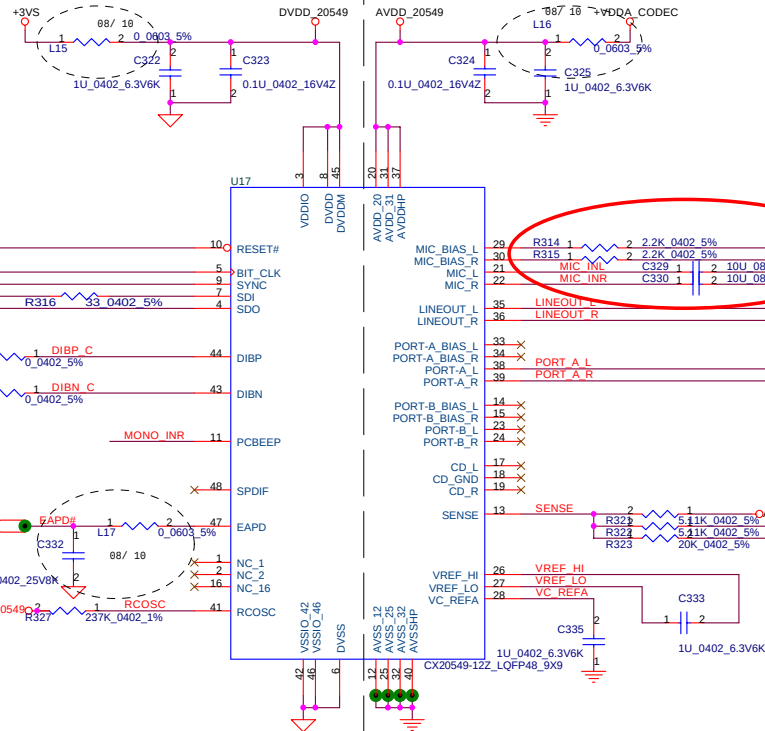
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				LA-3491P	
				Date	Rev
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CODEC POWER



AUDIO CODEC

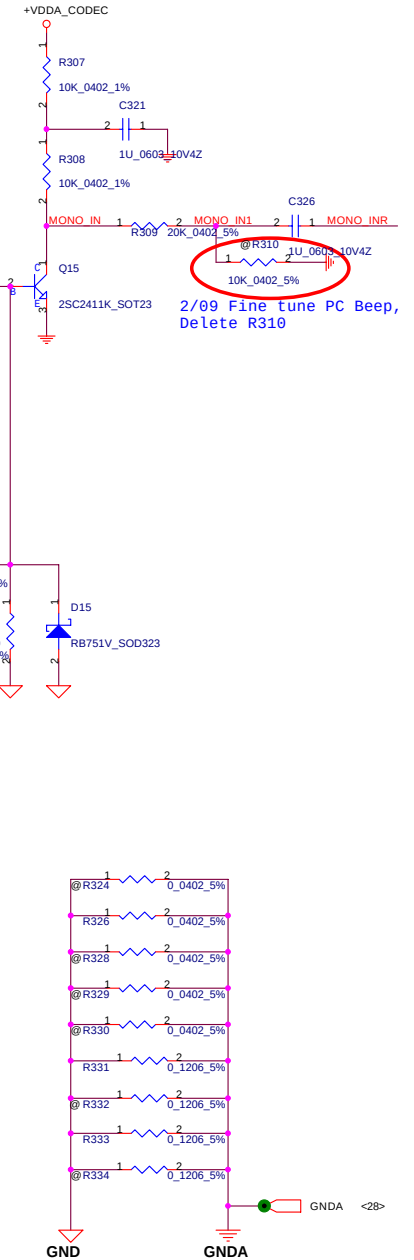
In order for the modem wake on ring feature to function, the CODEC must be powered by a rail that is not removed when the system is in standby.



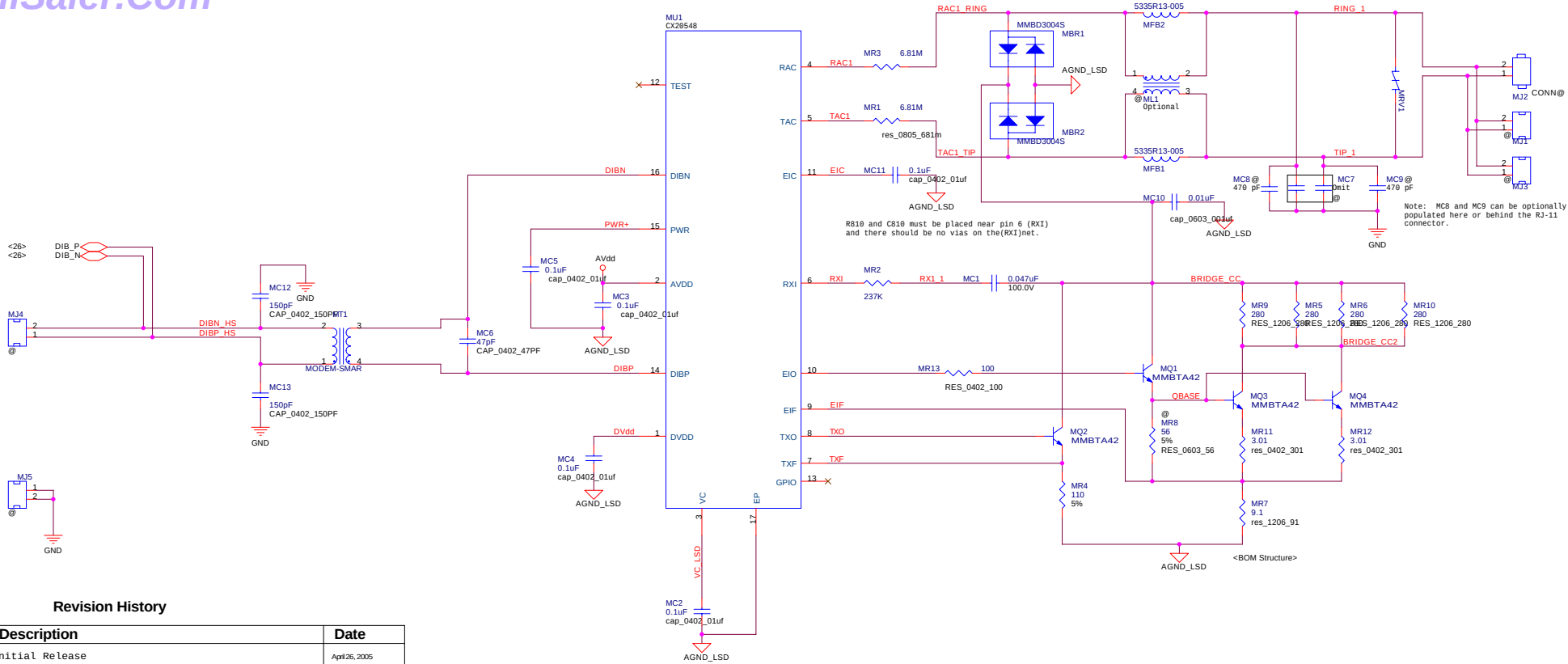
DIGITAL

ANALOG

03/10 Delete CBS de-pop circuit
03/20 Add CBS de-pop circuit, Change Q43 from FET to BJT



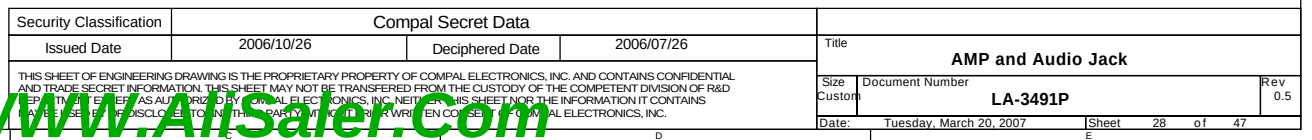
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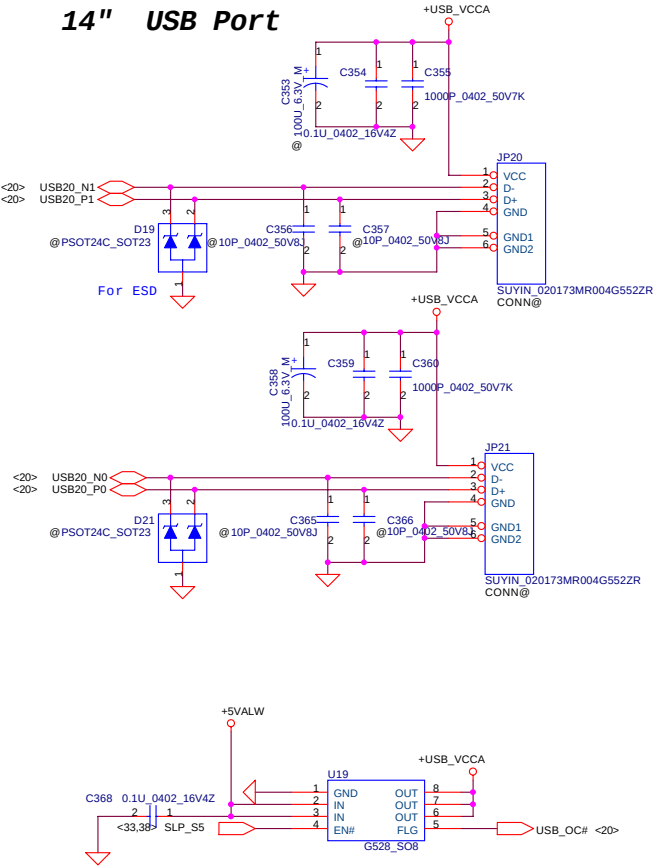
Revision History

REV	Description	Date
0	Initial Release	April 26, 2005
1	No changes to schematic. PCB updated to -003. Updated footprints and corrected via spacing errors.	August 18, 2005
2	Changed MC8 and MC9 pads. No schematic changes. PCB updated to -005.	November 3, 2005
3	Added MR11 and MR12. PCB updated to -007.	November 18, 2005
4	Added MR13. PCB updated to -009.	January 3, 2006
4.01	AVL update only.	April 20, 2005

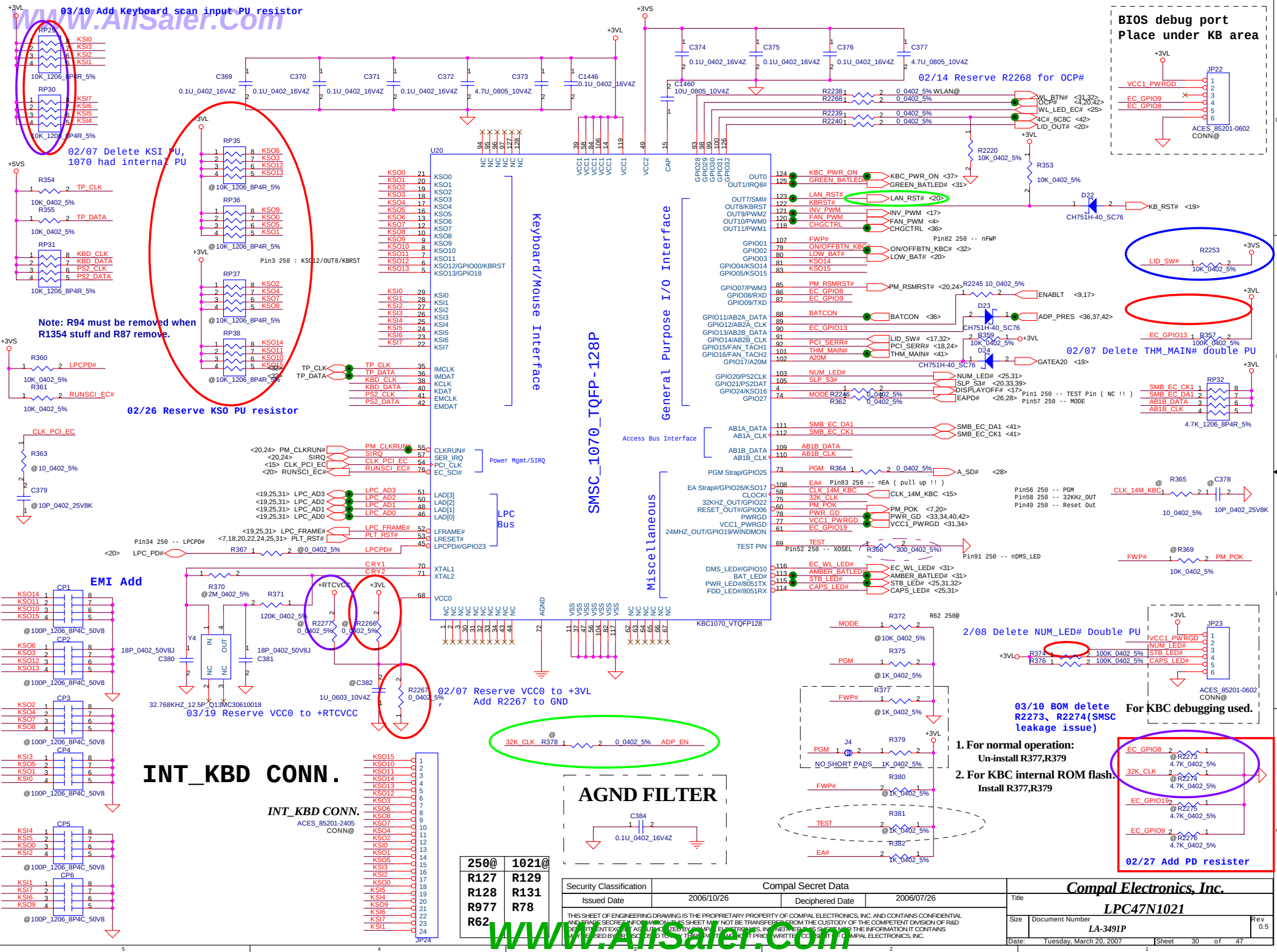
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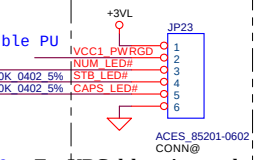
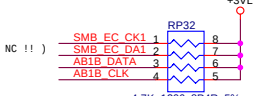
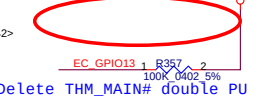
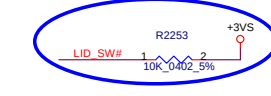
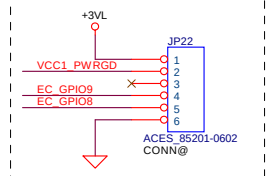
14" USB Port



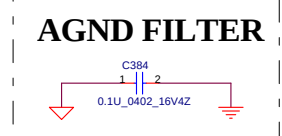
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Issued Date	2006/10/26	Deciphered Date	2006/07/26	Title		
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BIOS debug port
Place under KB area



- 1. For normal operation:
Un-install R377,R379
- 2. For KBC internal ROM flash:
Install R377,R379



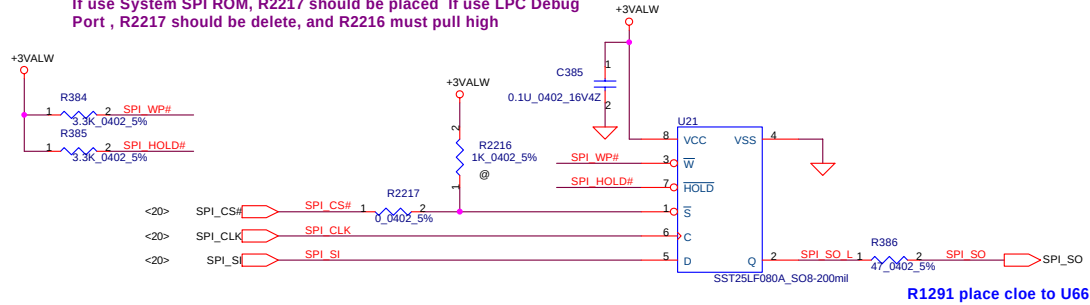
250@	1021@
R127	R129
R128	R131
R977	R78
R62	

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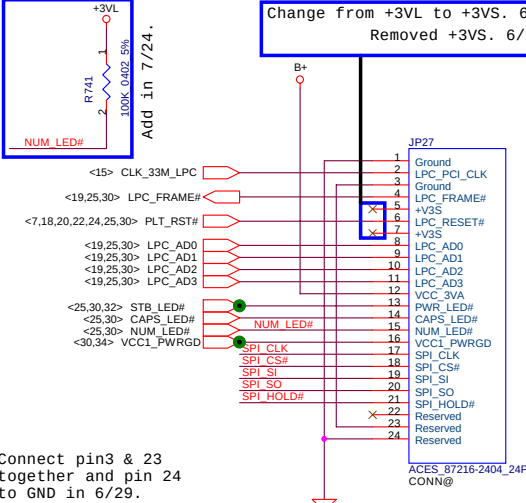
Compal Electronics, Inc.			
LPC47N1021			
Title	Document Number	Rev	0.5
Date	Tuesday, March 20, 2007	Sheet	30 of 47

BIOS ROM

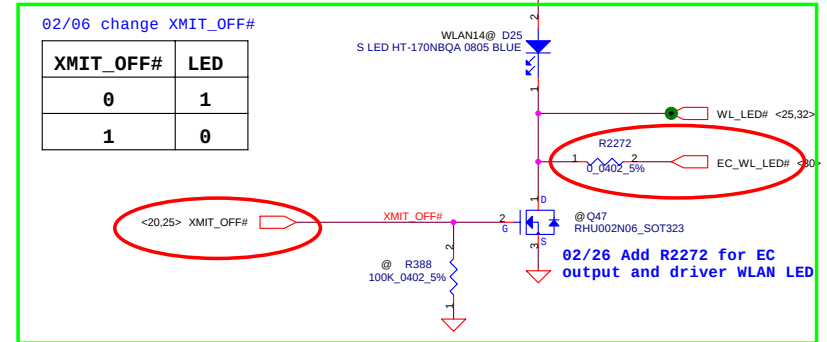
If use System SPI ROM, R2217 should be placed If use LPC Debug Port, R2217 should be delete, and R2216 must pull high



LPC Debug Port



Wireless LED BLUE

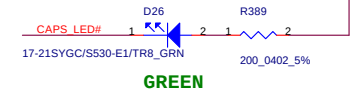


*WLAN LED Control note

WLAN have 3 ways control, the table list componet must be stuff

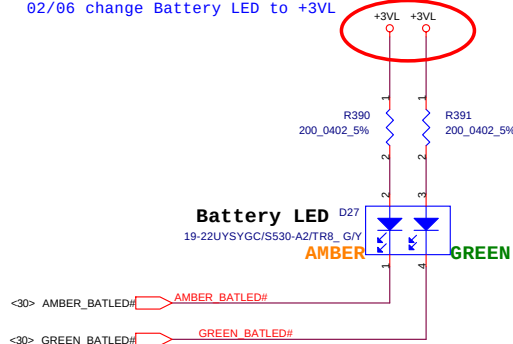
1	WLAN Card	R2263
2	XMIT_OFF#	R388 BQ47
3	EC control	R2270, R2271, R2272

CAP LED

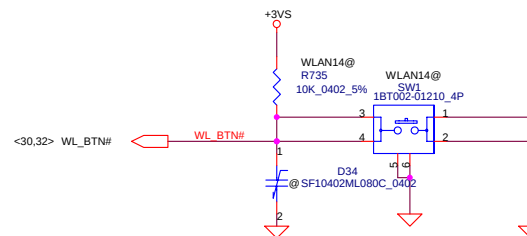


Charge LED

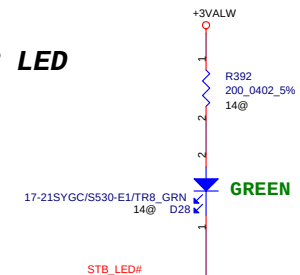
02/06 change Battery LED to +3VL



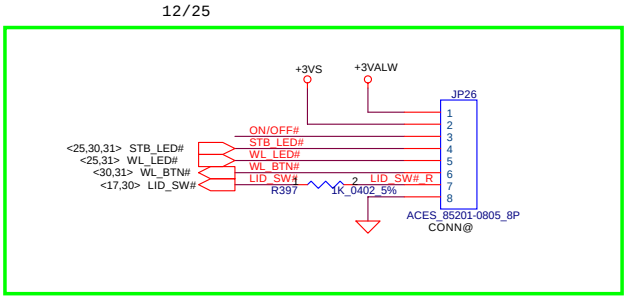
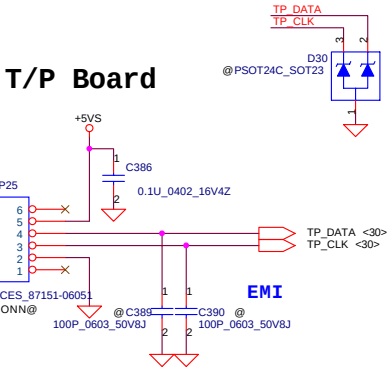
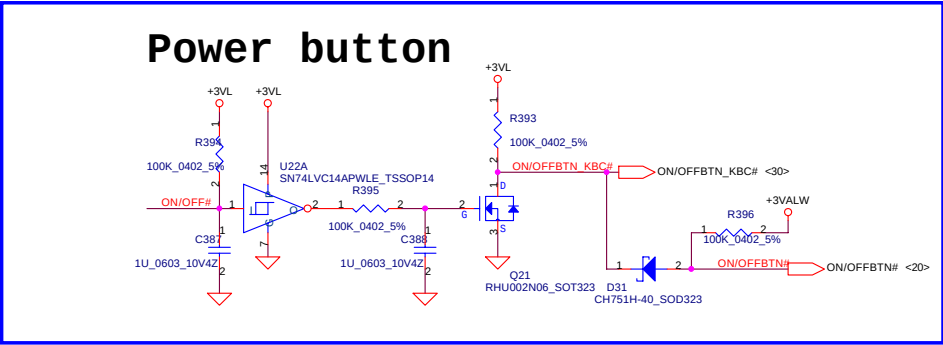
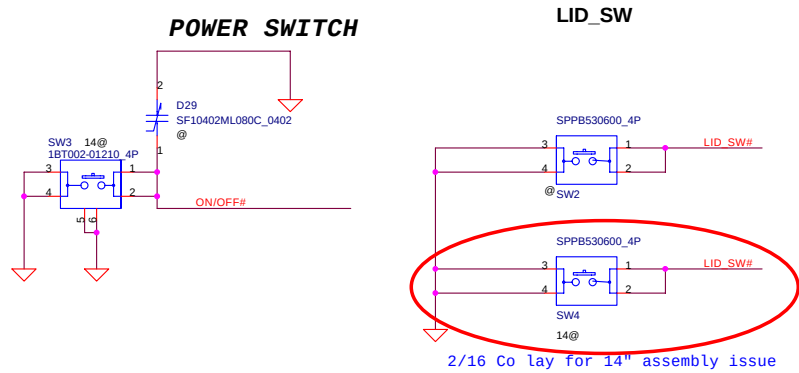
WL ON/OFF



POWER LED

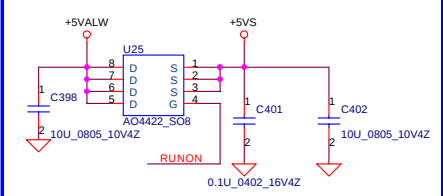


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				BIOS ROM/PS2/LED/SW			
Size		Document Number		LA-3491P		Rev 0.5	
Date		Tuesday, March 20, 2007		Sheet 31		of 47	

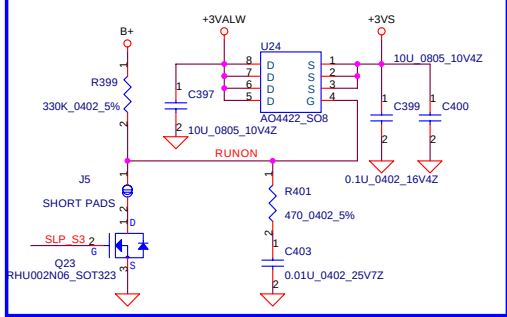


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Date:				Tuesday, March 20, 2007	Sheet 32 of 47

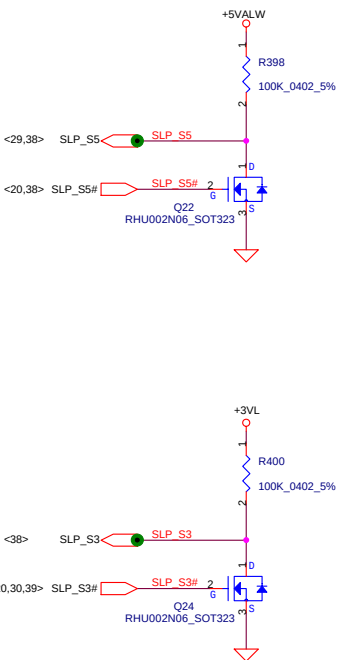
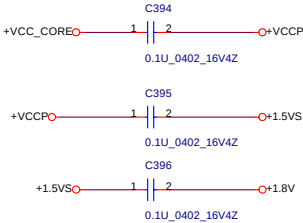
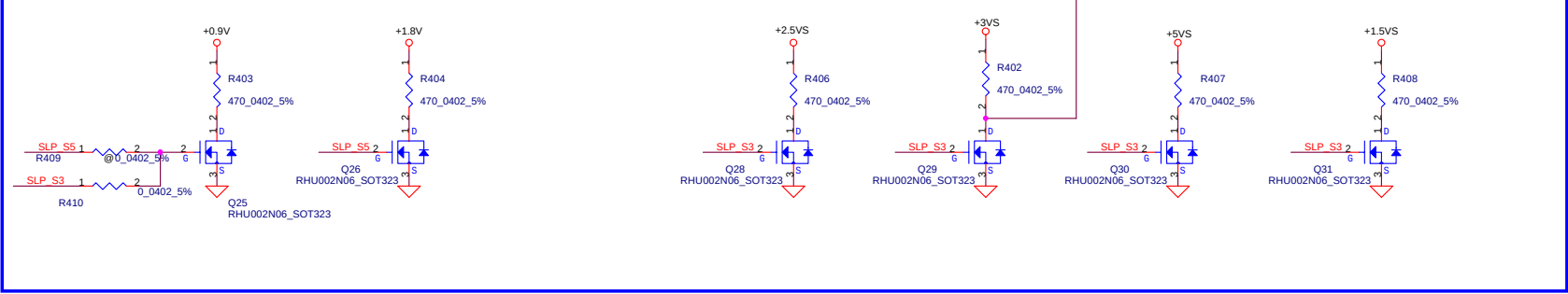
+5VALW to +5VS Transfer



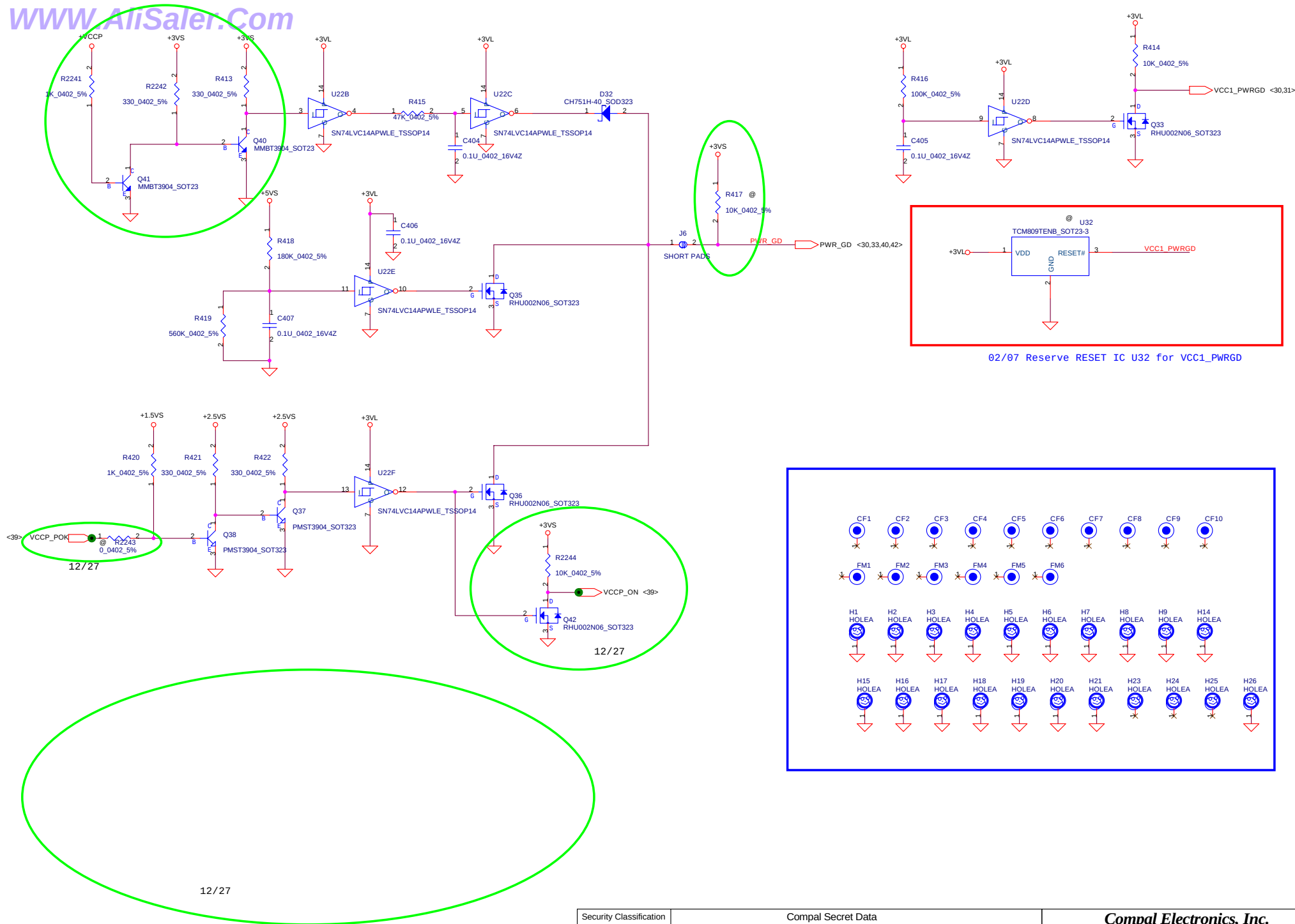
+3VALW to +3VS Transfer



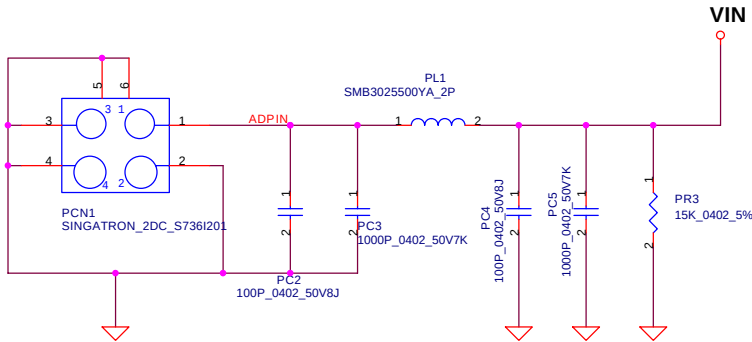
Discharge circuit



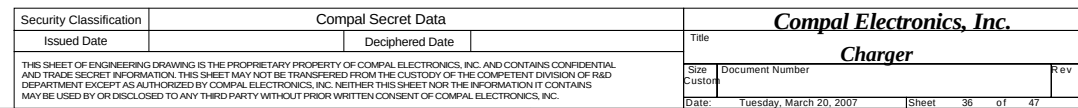
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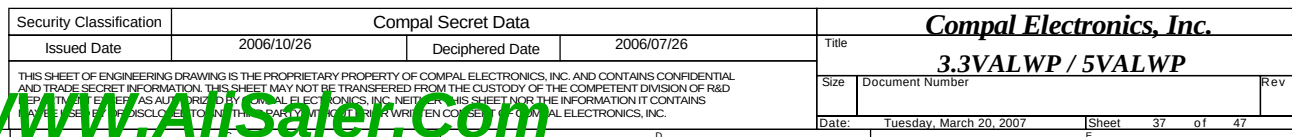


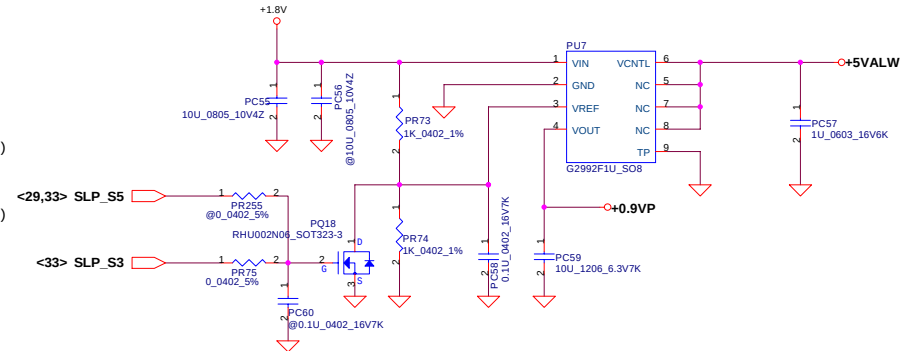
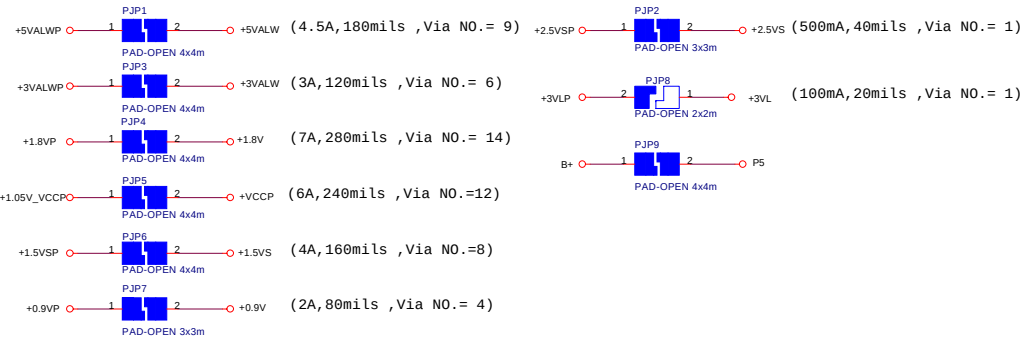
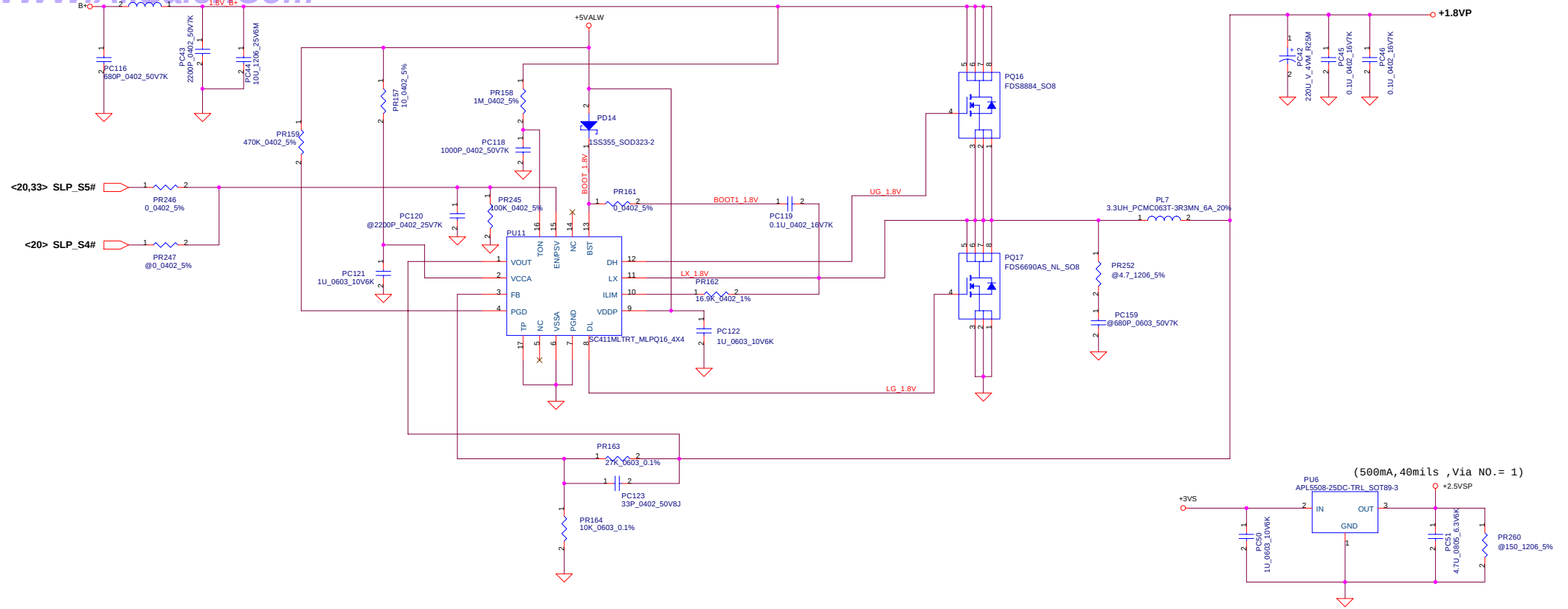
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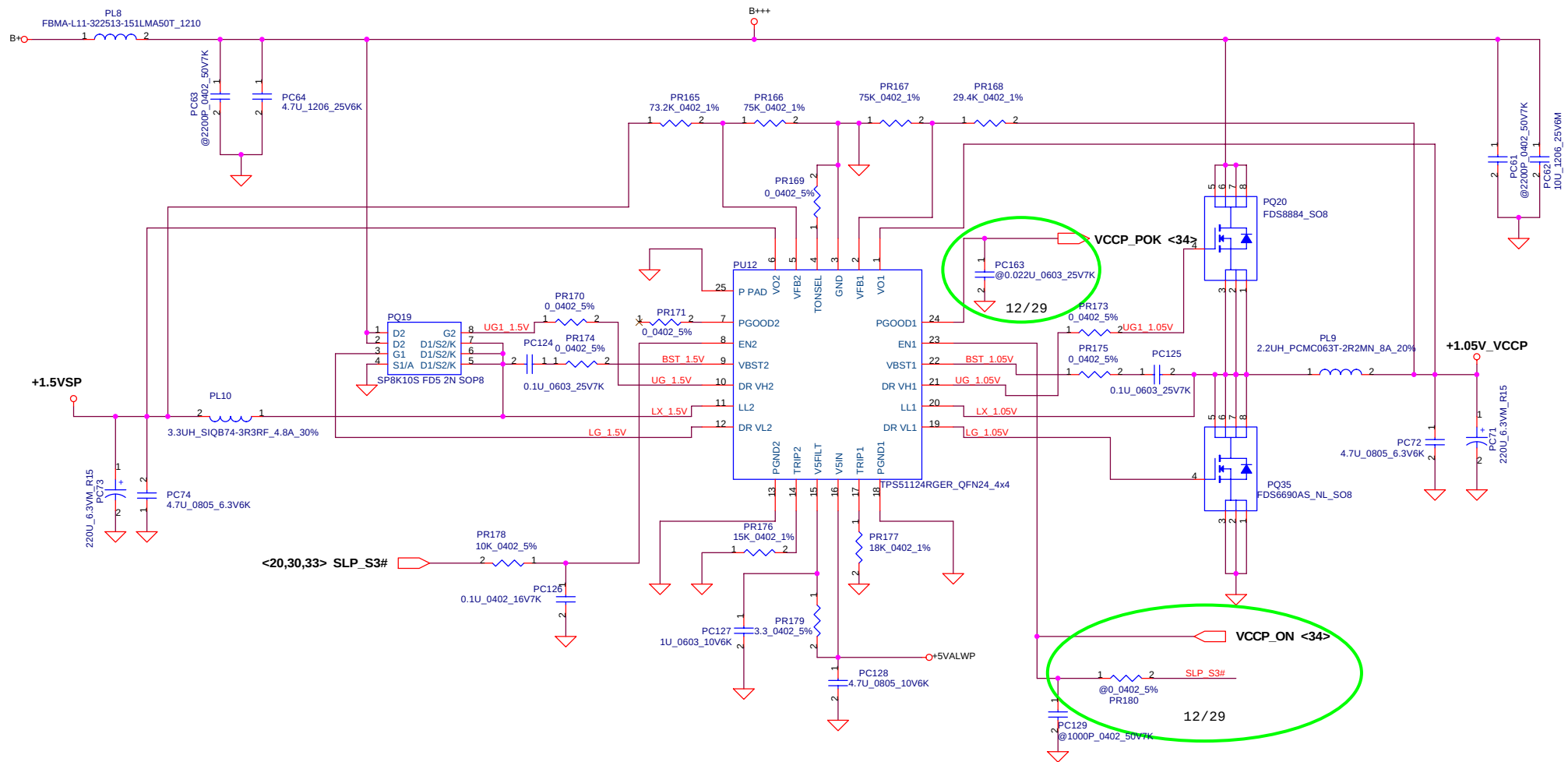
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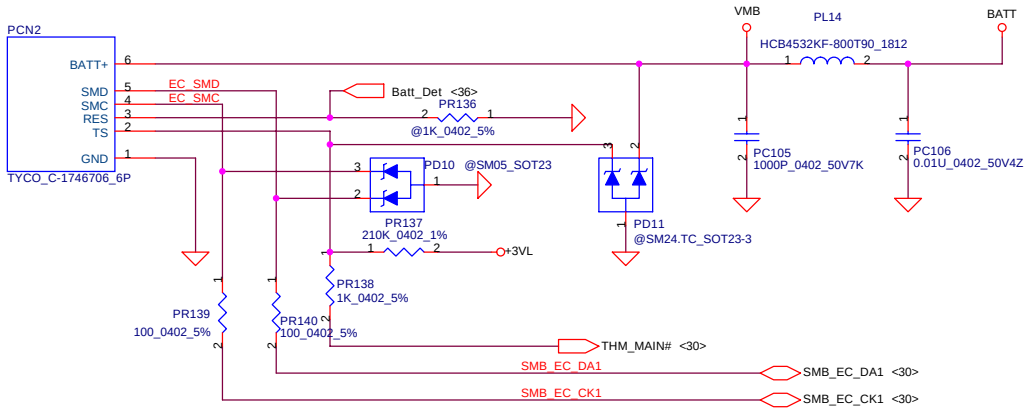




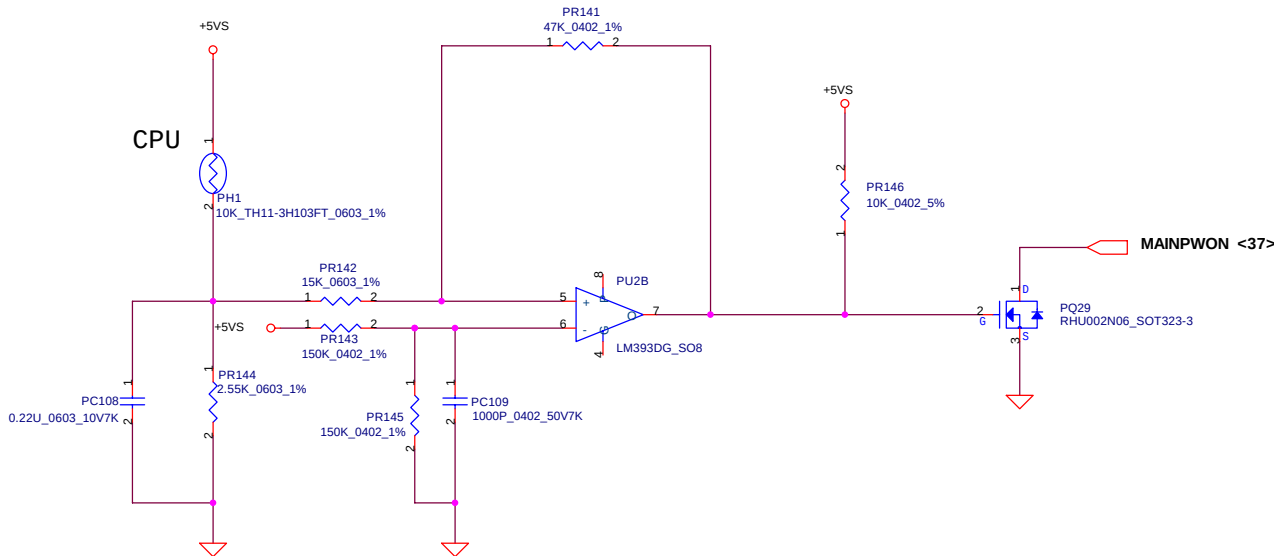
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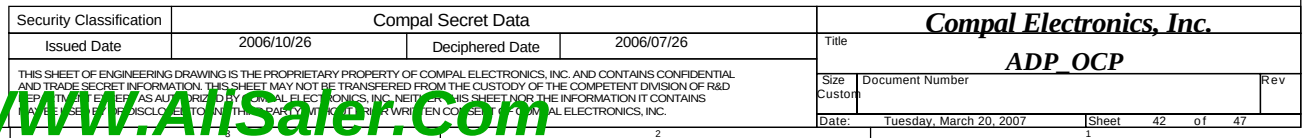
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PH1 under CPU botten side :
CPU thermal protection at 90 +-3 degree C
Recovery at 47 +-3 degree C



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Item	Reason for change	PG #	Modify List	Date	Phase
1	Reserve Disable TV-out power plane resistor	Page 10	Add R2221、 R2222、 R2223、 R2224、 R2225 for Disable TV-out power plane	01/02	DB2
2	R2211、 R2212 Change to 10k follow datasheet	Page 9	Change R2211、 R2212 to 10K_0402_5%	01/02	DB2
3	Disable TV-out follow datasheet	Page 9	Add resistor to +1.5VS power TVDAC_A(R2172)、 TVDAC_B(R2173)、 TVDAC_C(R2174)、 TV_IREF(R57) BTVIRTNA、 TVIRTNB、 TVIRTNC(R2251)	01/02	DB2
4	Change CPU and NB BCLK follow heavenly2.0	Page 15	CPU --->CPUCLKT0/C0 NB --->CPUCLKT1/C1	01/02	DB2
5	Change Mini card CLK From SRC3 to SRC7	Page 15	Change to SRC7	01/02	DB2
6	CRT connector PCB footprint error	Page 16	Change JP6 PCB Footprint form SUYIN_070912FR015S207CR_15P to ALLT0_C10510-115A5-L_15P	01/02	DB2
7	+ENAVDD add a 100k Pull low follow datasheet	Page 17	Add R2247 to GND	01/02	DB2
8	LCDVDD enable timing	Page 17	Change R159 to 47k、 C213 to 0.1u	01/02	DB2
9	Change AND gate that one gate one chip	Page 18	Change U28(4 in 1) to U30、 U31	01/02	DB2
10	Reserve EE PROM power plane +3VS	Page 19	Reserve R2230 for don't support wake up LAN Reserve R2231 for support wake up LAN	01/02	DB2
11	Add R2213 and verify need or not?	Page 19	Add R2213	01/02	DB2
12	Change PCIE from port 1 to port 2 follow caymus	Page 20 Page 25	Change MINI Card PCIE from Port 1to Port2	01/02	DB2
13	Reserve LAN_RST# that can fine tune from EC	Page 20 Page 30	Reserve R2233 for fine tune LAN_RST# timing	01/02	DB2
14	Change R to RP , keep original design	Page 20	Change to RP33、 RP34	01/02	DB2
15	Reserve +3VS power plane for don't support wake up LAN	Page 21	If R2237 --->support wake up LAN If R2236 --->Don't support wake up LAN	01/02	DB2
16	Reserve +3VALW power plane to verify HDA codec	Page 21	If R2234 --->AC97 codec If R2235 --->HD Codec	01/02	DB2
17	Reserve +3VALW power plane support wake up LAN	Page 23	If L11 --->Don't support wake up LAN If L20 --->Support wake up LAN	01/02	DB2
18	Reserve +3VALW power plane support wake up LAN	Page 24	If L12、 L13 --->Don't support wake up LAN If L21、 L22 --->Support wake up LAN	01/02	DB2
19	Reserve 0 ohm resistor for SMSC1070	Page 30	Reserve R2238、 R2239、 R2240	01/02	DB2
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Item	Reason for change	PG #	Modify List	Date	Phase
20	Wireless LED design issue	Page 31	Delete Q20	01/02	DB2
21	Change POK circuit form PG00D to VCCP_ON	Page 34	Add R2244、Q42, and reserve R2243	01/02	DB2
22	LID_SW# add 10k pull high	Page 30	Add R2253 for LID_SW# pull high	01/16	SI
23	Change use EAPD# to control Amp Shutdown	Page 28	Reserve R2198 and add R2252 pull high	01/16	SI
24	Change Battery LED power from +3VALW to +3VL	Page 31	Change Battery LED power from +3VALW to +3VL	02/06	PV
25	XMIT_OFF# control error	Page 31	Delete Q46	02/06	PV
26	Delete KSI PU, 1070 had internal PU	Page 30	Delete RP29、RP30	02/07	PV
27	Reserve SMSC 1070 VCC0 to +3VL,Add R2267 to GND	Page 30	Reserve R2266 to +3VL,Add R2267 to GND	02/07	PV
28	Change Codec Mix Resistor from 20k to 1k	Page 28	Change R2264、R2265 to 1K	02/07	PV
29	Change LAN82562GT RBIAS resistor to 649 ohm	Page 23	Change R274 to 649 ohm	02/07	PV
30	Reserve RESET IC for VCC1_PWRGD	Page 34	Reserve RESET IC U32 for VCC1_PWRGD	02/07	PV
31	THM_MAIN# Double pull high	Page 30	Delete R356	02/07	PV
32	Fine tune PC Beep	Page 26	BOM delete R310	02/09	PV
33	Change Hp series resistor to 60 ohm 0603	Page 28	Change R341、R343 to 60 ohm 0603	02/14	PV
34	Reserve OCP# to EC GPIO29(pin 98)	Page 30	Reserve R2268 to EC GPIO29(pin98)	02/14	PV
35	HP、MIC ESD Diode change to AGND	Page 28	HP、MIC ESD Diode change to AGND	02/14	PV
36	HP de pop when boot	Page 28	Add inverter to prevent HP pop noise	02/26	PV
37	C43、C44、C45 impact ME parts	Page 06	Change CPU core decoupling capacitor height limit 1.9mm for short term solution(SGA19331D00)	02/26	PV
38	WLAN LED use XMIT_OFF# have error beheive	Page 25 Page 30 Page 31	02/26 Add R2270 for WL_LED_EC# PU 02/26 Add R2271 for use EC detect WLAN active 02/26 Add R2272 for EC output and driver WLAN LED	02/26	PV
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Item	Reason for change	PG #	Modify List	Date	Phase
1	The PR172 changes to HW side	39	Remove PR172	2006/12/29	DB2
2	Change the +1.05V_VCCP power sequence	39	Remove PR180	2006/12/29	DB2
3	The +1.05V_VCCP dynamic range is over spec.	39	Change PL9 from 3.3UH to 2.2UH	2007/01/03	DB2
4	Adjust +1.5VSP voltage range	39	Change PR165 from 75K_ohm to 73.2K_ohm	2007/01/03	DB2
5	Change the PD18 diode	36	Change PD18 from 1SS355 to RLS4148	2007/01/16	SI
6	Change the +3VALWP output capacitor.	37	Change PC38 from 150U_D2_6.3VM to 220U_6.3V_R15	2007/01/16	SI
7	Change the +0.9VP output capacitor.	38	Change PC59 from 22U to 10U	2007/01/16	SI
8	Change the +1.05V_VCCP output capacitor.	39	Change PC71 from 220U_V_4VM_R25M to 220U_6.3V_R15	2007/01/16	SI
9	Change the +1.5VSP output capacitor.	39	Change PC73 from 220U_6.3VM_R15 to 220U_6.3V_R15	2007/01/16	SI
10	Change the +1.5VSP choke size.	39	Change PL11 from 3.3UH_PCMC063T-3R3MN_6A_20% to 3.3UH_SIQB74-3R3RF_4.8A_30%	2007/01/16	SI
11	Change PD14 diode	38	Change PD14 from CH751H-40PT to 1SS355	2007/02/05	PV
12	Adjust PU3 operation current	36	Change PR38 from 75K_ohm to 60.4K_ohm	2007/02/05	PV
13	Change PC25 capacitor.	36	Change PC25 form .022U to 22P	2007/02/05	PV
14	Change the +1.5VSP power sequence	39	1. Change PR178 form 0_ohm to 10K_ohm 2. Add PC126 0.1U	2007/02/05	PV
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